ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-2251

Design Guide for the Packaging of High Speed Electronic Circuits

IPC-2251
November 2003

Supersedes IPC-D-317A
January 1995

A standard developed by IPC

2215 Sanders Road, Northbrook, IL 60062-6135
Tel. 847.509.9700 Fax 847.509.9798
www.ipc.org

IPC

ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-2251

Design Guide for the Packaging of High Speed Electronic Circuits

Developed by the IPC-2251 Task Group (D-21a) of the High Speed/High Frequency Committee (D-20) of IPC

Supersedes:

IPC-D-317A - January 1995
IPC-D-317 - April 1990

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
2215 Sanders Road
Northbrook, Illinois
60062-6135
Tel 847 509.9700
Fax 847 509.9798

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the IPC-2251 Task Group (D-21a) of the High Speed/High Frequency Committee (D-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

A special note of gratitude goes to Philip R. Wellington of L-3 Communications and Nicholas G. Paulter of NIST for their invaluable contributions towards the development of this document.

High Speed/High Frequency Committee	IPC-2251 Task Group	Technical Liaisons of the IPC Board of Directors
Chair Thomas Bresnan R&D Circuits	Chair Byron Case L-3 Communications	Nilesh S. Naik Eagle Circuits Inc. Sammy Yi Flextronics International

IPC-2251 Task Group

Amit Bhardwaj, Polar Instruments (AP) Pte. Ltd.

Dr. Eric Bogatin, Giga Test Labs

Robert Bremer, Litton Systems Inc.

Christine R. Coapman, Delphi Delco Electronics Systems

David J. Corbett, Defense Supply Center Columbus

Theodore Edwards, Dynaco Corp.

Werner Engelmaier, Engelmaier Associates, L.C.

Martyn Gaudion, Polar Instruments Limited

Michael R. Green, Lockheed Martin Space Systems Company

Richard P. Hartley, C.I.D., Hartley Enterprises

Phillip E. Hinton, Hinton 'PWB' Engineering

David H. Hoover, Multek

Michael Jouppi, Thermal Man, Inc.

Thomas E. Kemp Rockwell Collins

George T. Kotecki, Northrop Grumman Corporation

Rene R. Martinez, Northrop Grumman

Deepak K. Pai, C.I.D.+, General Dynamics-Advanced Information

Nicholas G. Paulter, NIST

Mohammad Rahnavard, Xerox Corporation

John Reynolds, Rogers Corporation

Lowell Sherman, Defense Supply Center Columbus

Ken Taylor, Polar Instruments, Inc.

Daniel Welch, Arlon MED

Philip R. Wellington, L-3 Communications

Shlomi Zigdon, B.Sc., C.I.D., Shlomi Zigdon Technologies Ltd.

Table of Contents

1 GENERAL 1
1.1 Purpose 1
1.2 Scope 1
1.3 Symbology, Terms and Definitions 1
1.3.1 Symbology 1
1.3.2 Terms and Definitions 2
1.4 Units 6

2 APPLICABLE DOCUMENTS 6

3 OVERVIEW 6
3.1 Decision Making Process 6
3.2 Design Options 7
3.2.1 System Electrical/Mechanical Constraints 7
3.2.2 Signal Integrity Design Constraints 8
3.2.3 System Electrical/Mechanical Requirements 9
3.3 Mechanical Requirements 9
3.3.1 Circuit Board 10
3.3.2 Hybrid 10
3.3.3 Component Packaging 10
3.3.4 Thermal Management 10
3.3.5 Component Mounting 10
3.4 Electrical Considerations 10
3.4.1 Power Distribution 10
3.4.2 Permittivity 10
3.4.3 Capacitive Versus Transmission Line Environment 11
3.4.4 Propagation Time 11
3.4.5 Characteristic Impedance 11
3.4.6 Signal Loading Effects 11
3.4.7 Crosstalk 12
3.4.8 Signal Attenuation 12

4 MECHANICAL CONSIDERATIONS 12
4.1 Printed Board 12
4.1.1 Substrate Materials 12
4.2 Component Packaging 14
4.2.1 Device 14
4.2.2 Connectors 14
4.2.3 Cables 15
4.3 Thermal Considerations 15
4.3.1 System Level Impacts 15
4.3.2 Board Level Impacts 15
4.3.3 Device Level Impacts 16
4.4 Component Placement 17
4.4.1 Crosstalk Management 17
4.4.2 Impedance Control 17
4.4.3 Power Distribution 18
4.4.4 Thermal Management 18
4.4.5 System Cost 18

5 ELECTRICAL CONSIDERATIONS 18
5.1 Power Distribution 18
5.1.1 System DC Model 18
5.1.2 Power Plane Impedance 19
5.1.3 Integrated Circuit Decoupling 20
5.1.4 Decoupling Capacitance and Plane Capacitance 22
5.1.5 Device Power Dissipation 25
5.2 Permittivity 25
5.2.1 Relative Permittivity 25
5.2.2 Effective Relative Permittivity 25
5.2.3 Frequency Dependance 26
5.3 Lumped Capacitance Versus Transmission Line Environment 28
5.4 Propagation Delay Time 30
5.4.1 Capacitive Line 30
5.4.2 Transmission Line 30
5.5 Impedance Models 31
5.5.1 Microstrip 31
5.5.2 Embedded Microstrip 32
5.5.3 Centered Stripline 33
5.5.4 Dual-Stripline 33
5.5.5 Differential Pair Conductors 34
5.6 Loading Effects 36
5.6.1 Termination Resistors 36
5.6.2 Reflections 36
5.6.3 Minimum Separation 36
5.6.4 Distributed Loading 38
5.6.5 Lumped Loading 39
5.6.6 Radial Loading 40
5.6.7 Logic Signal Line Loading Models 41
5.6.8 Timing Calculation 42
5.7 Crosstalk 44
5.7.1 Model 44
5.7.2 Microstrip Transmission Line 46
5.7.3 Embedded Microstrip Transmission Line 46
5.7.4 Backward Crosstalk Amplitudes 46

5.7.5 Stripline ... 46
5.7.6 TTL/MOS Models ... 47
5.8 Signal Attenuation ... 47
5.8.1 Resistive Losses (Skin Effect) ... 47
5.8.2 Dielectric Losses ... 48
5.8.3 Rise Time Degradation ... 48
5.9 Computer Simulation Program ... 49
5.9.1 Computer Simulation Models ... 49
5.10 Connectors ... 49
5.10.1 Sensitivity ... 49
5.10.2 Distributed Line Compensations ... 49
5.10.3 Connector Types ... 49
5.11 EMI Layout Considerations ... 49
5.11.1 Reasons for Considering EMI Layout ... 49
5.11.2 Digital Edge Rates ... 50
5.11.3 Suggested EMI Layout Practices ... 50

6 PERFORMANCE TESTING ... 52
6.1 Impedance Testing ... 52
6.1.1 Principle of Impedance Testing Using a TDR ... 52
6.1.2 Impedance Measuring Test Equipment ... 52
6.2 Impedance Test Structures and Test Coupons ... 52
6.2.1 Test Structure Design ... 52
6.2.2 Test Probes and Connections ... 53
6.2.3 Locating Impedance Test Structures ... 53
6.2.4 A Simple Impedance Test Method ... 53
6.3 Stripline Impedance Test Coupon ... 53

Appendix A ... 55

Appendix B ... 76

Appendix C ... 80

Appendix D ... 82

Figures

Figure 3-1 High-Speed Packaging Design Concept ... 7
Figure 4-1 Schematic of Information, Electrical Power and Enthalpy (Heat) Flows ... 16
Figure 4-2 Heat Flux vs. Component Area ... 16
Figure 4-3 Component Placement Guideline ... 17
Figure 5-1 DC Distribution Model ... 18
Figure 5-2 DC Power Distribution System (Without Remote Sensing) ... 20
Figure 5-3 Decoupling Impedance Modeling - Power Supply ... 20
Figure 5-4 Device Decoupling Model ... 21
Figure 5-5 Capacitive and Transmission Line Current Pulses – A) is for a very short line and B) is for a long line ... 21
Figure 5-6 Fourier Transform ... 22
Figure 5-7 Capacitor Equivalent Circuit ... 23
Figure 5-8 (a) through (m) Typical Impedance Structures ... 27
Figure 5-9 ε_r and tan δ versus frequency for FR-4 ... 28
Figure 5-10 Capacitive Loading ... 30
Figure 5-11 Wire Over Reference Plane ... 31
Figure 5-12 Flat Conductor Surface Microstrip ... 32
Figure 5-13 Flat Conductor Embedded Microstrip ... 32
Figure 5-14 Flat Conductor Centered Stripline ... 33
Figure 5-15 Wire Conductor Centered Stripline ... 33
Figure 5-16 Flat Conductor Dual Stripline (Asymmetrical Signals) ... 34
Figure 5-17 Wire Conductor Differential Centered Stripline ... 34
Figure 5-18 Flat Conductor Shielded Broadside Coupled Differential Stripline ... 35
Figure 5-19 Flat Conductor Nonshielded Broadside Coupled Differential Stripline ... 35
Figure 5-20 Flat Conductor Shielded Edge Coupled Differential Stripline ... 35
Figure 5-21 Flat Conductor Shielded Edge Coupled Differential Dual Stripline ... 35
Figure 5-22 Flat Conductor Edge Coupled Differential Surface Microstrip ... 36
Figure 5-23 Flat Conductor Edge Coupled Differential Embedded Microstrip ... 36
Figure 5-24 Net Illustrating Point Discontinuity Waveforms ... 37
Figure 5-25 Addition of Two Pulses Traveling Opposite Directions ... 37
Figure 5-26 Distributed Line ... 38
Figure 5-27 Lumped Loading ... 39
Figure 5-28 Short Distributively Loaded Cluster ... 39
Figure 5-29 a) Lumped Loaded Transmission Line b) Equivalent Model ... 39
Figure 5-30 Waveforms for a Lumped Capacitive Load ... 39
Figure 5-31 Lumped Transmission Line ... 40
Figure 5-32 Radial Loading ... 40
Figure 5-33 Example Configuration ... 40
Figure 5-34 Example of Radial Line ... 41
Figure 5-35 Net Configuration ... 41
Figure 5-36 Bus Configuration ... 41
Figure 5-37 Wired-AND Configuration ... 42
Figure 5-38 Multiple Reflections in A Transmission Line Between Two TTL Inverters ... 43
Figure 5-39 Equivalent Circuit Example (top) with Corresponding Lattice Diagram (bottom) ... 44
Figure 5-40 Predicted Driver (A) and Load (B) Waveforms for Figure 5-39 ... 44
Figure 5-41 Induced Crosstalk Voltages ... 45

Figure 5-42 Crosstalk Voltages for a Line Terminated at Both Ends 45

Figure 5-43 Drivers and Receivers at a Common End 47

Figure 5-44 Drivers and Receivers at Opposite Ends 47

Figure 5-45 AC Noise Immunity for Selected TTL Families 48

Figure 6-1 TDR Impedance Test Coupon 54

Figure 6-2 Test Setup for Measuring Conductor Impedance (Suitable for Receiving Inspection) 54

Tables

Table 4-1 Wire Resistivity 13

Table 5-1 Copper Wire Characteristics 19

Table 5-2 Copper Busbar Resistances/ft 19

Table 5-3 Impedance for 0.1 µF and 0.001 µF DIP and 1206 Capacitors 23

Table 5-4 Typical Data for Some Logic Families 29

Table 5-5 Logic Model Classifications 36

Table 5-6 Connector Equivalent Bandwidth 50

Design Guide for the Packaging of High Speed Electronic Circuits

1 GENERAL

1.1 Purpose The object of this document is to provide guidelines for the design of high-speed circuitry. The subjects presented here represent the major factors that may influence a high-speed design. This guide is intended to be used by circuit designers, packaging engineers, circuit board fabricators, and procurement personnel so that all may have a common understanding of each area.

1.2 Scope The goal in electronic packaging is to transfer a signal from one device to one or more other devices through a conductor. Considerations include electrical noise, electromagnetic interference, signal propagation time, thermo-mechanical environmental protection, and heat dissipation. High-speed designs are defined as designs in which the interconnecting properties affect circuit function and require consideration. Every electrical concept has relevant physical implementation data and limitations provided to match the electrical and mechanical relationships. This guideline presents first order approximations for each of the subject areas covered. If more detail is required, the papers presented in the bibliography may provide more detailed supplemental data. Since most high speed design requires signal intergrity and EMI techniques, often field solvers, signal integrity simulation tools, EMI/EMC simulation programs may be required for resolving design challenges. Many PWB layout design tools include these tools as options to their programs. These simulators are driven by SPICE, IBIS, or other models. References to manufacturers of these tools may be found on the IPC Web site (www.ipc.org).

1.3 Symbology, Terms and Definitions

1.3.1 Symbology

Symbol	Description
ABT	Advanced Bipolar-CMOS Technology
AC	Advanced CMOS
AC	Alternating Current (Time varying current)
ACQ	Advanced CMOS Quiet
ACT	Advanced CMOS TTL Compatible
ACTQ	Advanced CMOS TTL Compatible Quiet
AGP	Advanced Graphics Port Logic
AHC	Advanced High-Speed CMOS
AHCT	Advanced High-Speed CMOS TTL Compatible
ALS	Advanced Low Power Schottky Technology
AS	Advanced Schottky Technology
BCT	Bipolar-CMOS Technology
CMOS	Complimentary Metal Oxide Semiconductor
COB	Chip-On-Board
CTE	Coefficient of Thermal Expansion
CTE_{XY}	X and Y-Axis Coefficient of Thermal Expansion
CTE_Z	Z-Axis Coefficient of thermal expansion
CTT	Center Tap Terminated Logic
DC	Direct Current
DIP	Dual In-line Package
DWB	Discrete Wiring Board
dV/dT	Delta Voltage/Delta Time (Edge Slew Rate)
ECL	Emitter Coupled Logic
EMI	Electromagnetic Interference
ESD	Electro-Static Discharge
F	Fast Bipolar Logic Technology
FR-4	Flame Retardant Level 4, Epoxy Glass Dielectric Material
GaAs	Gallium Arsenide Technology
GTL	Gunning Transceiver Logic
GTL+	Gunning Transceiver Logic Plus
HC	High-Speed CMOS Technology
HCT	High-Speed CMOS TTL Compatible
HL	High-to-Low Signal Edge Transition
HSTL	High-Speed Transceiver Logic
IBIS	I/O Buffer Information Specification
IBuf	Input Buffer
IC	Integrated Circuit
K_B	Backward Crosstalk
K_F	Forward Crosstalk
L_G	Ground Plane Inductance
L_H	Low-High Signal Edge Transition
L_P	Power Plane Inductance
LVDS	Low Voltage Differential Signalling
LVEL	Low Voltage ECL
LVPECL	Low Voltage PECL
LVCMOS	Low Voltage CMOS Technology
LVT	Low Voltage Technology

LVTTL	Low Voltage TTL Technology
LVX	Low Voltage CMOS Translation
OBuf	Output Buffer
PCI	Peripheral Component Interconnect
PDN	Power Distribution Network
PDS	Power Distribution System
PECL	Positive ECL Technology
PWB	Printed Wiring Board
R_C	Series Lead Resistance
R_G	Ground Plane Resistance
R_P	Power Plane Resistance
RSECL	Reduced Swing ECL
R_T	Sheet Resistance
Si-Ge	Silicon-Germanium
SM	Surface Mount
SPICE	Simulation Program with Integrated Circuit Emphasis
SSTL	Stub Series Terminated Logic
TAB	Tape Automated Bonding
Tan δ	Dissipation Factor (Loss Tangent)
TDR	Time Domain Reflectometer
t_f	10%-90% Edge Transition Time (Fall Time)
t_P	Total Signal Line Propagation Delay Time
t_{PD}	Propagation Delay Per Unit Length
t_r	10%-90% Edge Transition Time (Rise Time)
TTL	Transistor Transistor Logic
Z_O	Characteristic Line Impedance (Unloaded)
Z_O'	See 5.6.4
ε_r	Real Part of Relative Permittivity
$\varepsilon_{r,eff}$	Real Part of Effective Relative Permittivity
δ	Skin Depth

1.3.2 Terms and Definitions The terms listed below are used in this document. Their definitions are given in order to help the new reader. These definitions are also found in IPC-T-50, "Terms and Definitions for Interconnecting and Packaging Electronic Circuits." Where possible, definitions that appear in the body of this document are referred to as follows: "Bus - 5.6.7.2." This indicates that a definition for "Bus" appears in 5.6.7.2, and will not be repeated here.

AC Impedance – The combination of resistance, capacitive reactance, and inductive reactance experienced by time-varying voltage.

Alternating Current (AC) – A current that varies with time. This label is commonly applied to a power source that switches polarity many times per second, such as the power supplied by utilities. An AC signal may take a sinusoidal shape, but could be a square or triangular wave shape.

Amplitude – The difference between the high level and the low level of a voltage or current signal.

Analog Ground Plane – A solid copper or electrically conductive plane or plane-shape within a layer of a PWB. It provides a low inductive Analog ground signal reference (return path) for analog signal conductors on adjacent or buried layers. It also provides ground interconnect for analog active and passive analog devices.

Asymmetrical Dual-Strip Stripline – A stripline where the signal conductor that is embedded between two ground planes is not centered between them.

Attenuation – Reduction in the amplitude of a signal due to losses in the media through which it is transmitted.

Backward Crosstalk – Noise induced into a quiet line by an adjacent active line as seen at the end of the quiet line that is closest to the signal source. Typically, backward crosstalk is an inductive form of Crosstalk.

Broadside Coupled Pair – Signal conductors on adjacent layers that are routed parallel to each other, exhibits mutual trace-width coupled impedance between them, typically 50 to 150 ohms. Usually the conductors are matched in length or delay to a given tolerance.

Bulk Decoupling Capacitor – A capacitor that provides low frequency charge storage. Typically a tantalum or aluminum electrolytic dielectric capacitor placed at the power input of a circuit board and others distributed throughout the printed wiring board to reduce noise power and provide energy storage for high frequency decoupling capacitors.

Bus – See 5.6.7.2.

Busbar – A large copper or brass bar used to carry high power supply currents onto a printed wiring board (PWB) or backplane.

Capacitance – A measure of the ability of two adjacent conductors separated by an insulator to hold a charge when a voltage is impressed between them. Measured in Farads.

Characteristic Impedance – The vector sum of the impedance and reactance of a parallel conductor structure to the flow of AC current. Usually applied to transmission lines in printed boards and to cables carrying high-speed signals. Normally the characteristic impedance is a constant value over a wide range of frequencies and typically is referred to as Z_O.

Chassis Ground Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance reference (return path) for signal conductors on adjacent or buried conductors. The chassis ground plane may also be placed on the top and bottom layers of a printed wiring board to reduce electromagnetic emissions emanating from internal layers.

Circuit Board – For the purposes of this guideline the term circuit board covers both printed circuit board and discrete wiring boards where a circuit function is performed.

Clock – A gated synchronous or continuous digital periodic signal that provides timing for logic circuits.

Coaxial Transmission Line (Coax) – A transmission line structure where a round signal conductor is centered coaxially within a hollow cylindrical return (ground) conductor. The inside diameter of the return conductor is greater than the outside diameter of the signal conductor.

Crossover – Intersection of two conductors separated by dielectric.

Crosstalk – See 3.2 of Appendix B.

Current – The rate at which electrons travel in a conductor as a result of a voltage difference between the ends of the conductor. The unit of measure for current is the ampere, A.

Decoupling – Absorption or isolation of the noise that is induced in the power supply lines by switching logic devices. Decoupling prevents switching logic devices from disturbing other logic devices on the same power supply circuit. Decoupling is usually accomplished using capacitors (see 5.1.3).

Differential Impedance – The resistance of a dual parallel conductor structure to the flow of AC current. Usually applies to broadside coupled or edge coupled transmission lines in printed wiring boards and cables carrying high-speed signals. Differential impedance is normally a constant value over a wide range of frequencies and is typically referred to as Z_{DIFF}.

Differential Pair – Parallel routed signal lines exhibiting mutual coupled impedance between them that is typically between 50 ohms to 150 ohms. Usually the conductors are matched in length or delay to a given tolerance.

Direct Current (DC) – A current produced by a voltage source that does not vary with time. Normally provided by power supplies to power electronic circuits.

Discrete Wiring Board – Circuit board using round insulated wire to form signal paths that is terminated at both ends by a plated through hole.

Dissipation Factor – A parameter used to express the tendency of insulators or dielectrics to absorb some of the energy in an AC signal.

Dual Asymmetrical Stripline – A stripline signal conductor(s) that is embedded between two ground planes, and is not centered between them (closer to one ground plane than the other).

Edge Coupled Pair – Signal conductors routed parallel to each other on the same layer that exhibit mutual edge coupled impedance between both lines, typically between 50 ohms to 150 ohms. Usually the conductors are matched in length or delay to a given tolerance.

Edge Rate – The rate of change in voltage with time of a logic signal transition. Usually expressed in volts per nanosecond.

Edge Transition Attenuation – The reduction in the edge rate of a pulse caused by absorption of the higher frequency components of the pulse by the transmission line.

Effective Permittivity (Dielectric Constant) – See 5.2.2.

Effective Relative Permittivity – See 5.2.2.

Electromagnetic Interference (EMI) – Degradation of the performance of a device, equipment or system caused by an electromagnetic disturbance. Government regulating agencies control the allowable limits for radiated and conducted emissions surrounding electronic devices. Self-compatibility controls the allowable limits for internal radiated and conducted emission limits.

EMI Conducted Emissions – Conducted electromagnetic energy from digital, power, analog or components which is injected onto traces, power line conductors, or cables that cause interference to external or internal electronic circuitry. Often conducted EMI that is present on cables causes radiated EMI emissions in a system. Government regulating agencies control the allowable limits for radiated and conducted emissions surrounding electronic devices. Self-compatibility controls the allowable limits for internal radiated and conducted emission limits.

EMI Radiated Emissions – EMI that is the result of electromagnetic energy radiated from an electrical or electronic device, circuit or system. The Federal Communications Commission (a U.S. regulatory agency) and international technical and scientific organizations (such as the European Union - EU) limit the power of emissions radiated from electronic systems. Self-compatibility controls the allowable limits for internal radiated and conducted emission limits.

EMI Susceptibility – The sensitivity or vulnerability of an electronic device, circuit, or system to become adversely affected by radiated or conducted electromagnetic emissions. International and national technical and scientific organizations set upper limits on the energy or power levels (usually as a function of frequency) below which performance degradation of the device, circuit, or system should not occur. Self-compatibility of a system sets the maximum power levels for internally generated conducted and radiated emissions.

Electrostatic Discharge (ESD) – The resulting current field created when a high-voltage is discharged to a ground return. An ESD may follow multiple coupling paths (including sensitive circuitry) to ground creating radiated EMI emissions. ESD may cause circuit malfunction, failure, or damage depending on the circuit's ESD or EMI susceptibility.

ESD Damage – The damage caused to an electronic circuit when an unwanted high-voltage short-duration electrical pulse discharges into a static sensitive device. ESD damage often causes latent defects in semi-conductors. Generally, all semiconductors and some passive devices are ESD sensitive.

ESD Susceptibility – The vulnerability of a circuit to be affected by ESD. Typical ESD susceptibility tests are direct discharge and indirect discharge test based on the ESD established models.

Fall Time – Time required for a logic signal to switch from its high state to its low state. Commonly measured between the 90% and 10% aplitude levels. Transition duration is the term preferred and accepted by both international (IEC) and national (Institute of Electronic and Electrical Engineers, or IEEE) standards setting bodies to describe fall time. See IEC-469-1. IBIS Models commonly use dV/dT measured between the 20% and 80% voltage levels. See Transition Duration.

Flat Conductor – A rectangular conductor that is wider than it is high. Usually refers to signal conductors in a printed wiring board.

Forward Crosstalk – Noise induced into a quiet line placed next to an active line as seen at the end of the quiet line, which is farthest from the signal source. Typically Forward Crosstalk is a capacitive form of Crosstalk.

Ground – A term used to describe the terminal of a voltage source that serves as a measurement reference for all voltages in the system. Ground is often, but not always, the negative terminal of the power source.

Ground Bounce – A term used to describe the effect when multiple simultaneously switched outputs change from one state to another and which subsequently causes a quiet (undriven) input or output to follow the edges of the driven outputs (see 3.2.1.7). This effect is a difference of voltage drop between the die pad and the package-pin pad or leadframe.

Ground Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance ground reference (return path) for signal conductors on adjacent or buried lines. The ground plane also provides a ground connection for active and passive devices.

High-Frequency Decoupling Capacitor – A Capacitor that can charge/discharge high-frequency energy. Typically the high-frequency decoupling capacitor is a ceramic dielectric capacitor placed between the power pin and ground of an IC or discrete circuit to supply high frequency switching edge energy for the device or circuit. Multiple capacitors and/or values may be required for large IC packages.

IBIS Model – A model used for Signal Integrity analysis that defines a device's package parasitics, input characteristics, internal clamps, output characteristics, measurement thresholds, and edge rates. IBIS is not usually a proprietary model.

Impedance – The resistance to the flow of current represented by an electrical network. May be resistive or reactive, or both.

Inductance – The property of an electrical device or circuit that describes how well a time-varying current can induce an electromotive force in that or a nearby device or circuit. Inductance is proportional to the total magnetic flux and current through the device or circuit and its unit of measure is the Henry(H). Inductors store energy in a magnetic field.

Line Coupling – Coupling between two transmission lines caused by their mutual inductance and the capacitance between them.

Load Capacitance – The capacitance seen by the output of a logic circuit or other signal source. Load Capacitance is usually the sum of distributed line capacitance and input of the load circuits.

Logic – A general term used to describe the functional circuits used in computers and other digital electronics to perform computational or control functions.

Logic Family – A collection of logic functions or ICs using the same form of electronic circuit technology. Examples: ECL-Emitter Coupled Logic; TTL-Transistor-Transistor Logic; CMOS-Complimentary Metal Oxide Semiconductor logic; GTL-Gunning Transceiver Logic.

Microstrip – Microstrip, microstripline, and microstrip line are used interchangeably (see 5.5.1).

Net – See 5.6.7.1.

Nonmonotonic Edge (Transition) – A term used to describe an unwanted signal integrity "double edge" effect that occurs during a rising or falling edge, where two edges are generated (sometimes referred to as a double clock) (see 3.2.1.4).

Overshoot – The amount by which a pulse exceeds its nominal amplitude after its transition from one state to another. Overshoot is a signal aberration and is usually given as a percentage of the nominal pulse amplitude. Overshoot can be caused by pulse reflections from impedance discontinuities in a transmission line. Typically, the discontinuities that contribute to overshoot are from a low to high impedance. For example, the signal amplitude may temporarily rise to 6.5 V because of reflections even though the supply voltage is only 5.0 V (see 3.2.2.1).

Parallel Pair – Two conductors that are routed side by side on the same or on adjacent layers and are at a controlled separation.

Permeability – A general term used to express various relationships between magnetic induction and magnetizing force.

Permittivity (Dielectric Constant) – See 5.2.

Plane – A solid copper or electrically conductive layer or plane-shape within a layer of a PWB. Planes are typically used for power and ground distribution, impedance control, and circuit isolation. Planes may be voltages, grounds, digital, analog, RF circuitry, or whatever is required for the design. A PWB will generally have multiple plane layers or plane-shapes.

Power Distribution Network (PDN) – The network of power distribution elements on a PWB or system that delivers power from one location (source) to destination devices. The network is composed of inductive and capacitive elements. The PDN is designed to provide a low impedance source across applicable frequency range to destination devices. Also referred to as Power Distribution System (PDS).

Power Distribution System (PDS) – See Power Distribution Network (PDN).

Power Dissipation – Energy used by an electronic device in the performance of its function.

Power Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance reference for signal conductors on adjacent or buried layers and a power interconnect for active devices.

Power Plane Inductance – See 5.1.2.1.

Power Plane Coupled Noise – An unwanted signal integrity effect when edge-switching noise is transferred from one circuit to another through the power planes.

Printed Wiring Board – A circuit board utilizing etched copper traces for signal interconnections.

Propagation Delay – The time from output to input required for a signal to travel along a transmission line, or the time required for a logic device to receive an input stimulus, perform its function, and present a signal at its output.

Pulse – A logic signal that switches from one state to another and back in a short period of time, and remains in the original state most of the time. Usually used as timing strobe signals for logic devices.

Reflection – Energy from a high-speed signal edge that is sent back toward the source as a result of encountering a change in impedance in the transmission line on which it is traveling.

RF Ground Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance RF reference for analog signal conductors on adjacent or buried layers. The RF ground plane also provides a ground connection for active and passive RF devices.

Rise Time – Time required for a logic signal to switch from its low state to its high state. Commonly measured between the 10% and 90% voltage levels. Transition duration is the term preferred and accepted by international (IEC) and national (IEEE) standards setting bodies to describe rise time. See IEC-469-1. IBIS Models commonly use dV/dT measured between the 20% and 80% voltage levels. See Transition Duration.

Routed Signal Line Delay – See 3.2.1.6.

Signal Ground – The common ground return reference for logic signals. Typically one or more signal ground planes in a PWB.

Signal Ground Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance reference for digital signal conductors located on adjacent or buried layers. The signal ground plane also provides a ground connection for active and passive devices.

Signal Integrity Degradation – Signal aberrations that degrade system performance or cause mis-operation. These signal aberrations may be Overshoot, Undershoot, Crosstalk, Nonmonotonic edges, Ground bounce, Power plane coupled noise, or Routed signal line delay skew.

Signal Line – Any conductor used to transmit an electrical signal from one circuit to another.

Skin Effect – See 5.8.1.

SPICE Model – A model used for Signal Integrity analysis that defines a device's package parasitics, input characteristics, and output characteristics.

Stripline – See 5.5.3.

Stub – A branch of the main line of a signal net usually used to reach a load that is not on the direct signal path.

Matched Termination – A term used to describe the matching of the driving source, transmission media, and destination load to minimize signal integrity degrading effects.

Transition Duration – The difference between the instants on the same transition that the waveform crosses specified reference levels. Unless otherwise specified, the two *reference levels* are the 10% and 90% *reference levels.* IBIS Models commonly use dV/dT measured between the 20% and 80% voltage levels.

Deprecated Terms: Risetime, Falltime, Leading Edge, Rising Edge, Trailing Edge, Falling Edge, Transition Time – The terms *risetime, falltime,* and *transition time,* although widely used, are deprecated because they are ambiguous and confusing. First, the use of the word time in this standard refers exclusively to an *instant* and not an *interval*. Also, if the *first transition* of a *waveform* within a *waveform epoch* happens to be a *negative transition*, some users may refer to its *transition duration* as its *risetime*, and some others may refer to its *transition duration* as its *falltime*. If the use of these deprecated terms is required, then *risetime* is synonymous with the *transition duration* of a *positive-going transition*, and *falltime* is synonymous with the *transition duration* of a *negative-going transition*. If the upper and lower *state boundaries* of the two *states* are not the user-defined *reference levels* (for example, the 10% and 90% *reference levels*), then the *duration* of a *transition* is not equal to the *transition duration*. IBIS Models commonly use dV/dT measured between the 20% and 80% voltage levels.

Transmission Line – A signal-carrying circuit with controlled conductor and dielectric material physical relationships such that its electrical characteristics are suitable for the transmission of high frequency or narrow pulse electrical signals.

Undershoot – A term used to describe an unwanted signal integrity effect that occurs after successive reflections causing a short additional pulse within the supply or ground rails after the original transition (see 3.2.1.3).

Waveguide – A rectangular or round tube used to transmit RF energy in the form of an electromagnetic wave rather than as a current in a wire.

1.4 Units All dimensions and tolerances in this standard are expressed in hard metric (SI) units and parenthetical soft imperial (inch) units.

2 APPLICABLE DOCUMENTS[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-DW-424 General Specification For Encapsulated Discrete Wire Interconnections Boards

IPC-DW-425 Design End Product Requirements for Discrete Wiring Boards

IPC-2141 Controlled Impedance Circuit Boards and High Speed Logic Design

IPC-2221 Generic Standard on Printed Board Design

IPC-2223 Sectional Design Standard for Flexible Printed Boards

IPC-4103 Specification for Base Materials for High-speed/High Frequency Applications

IPC-4562 Metal Foil for Printed Wiring Applications

3 OVERVIEW

Packaging of electronic equipment has traditionally been an area for mechanical considerations. An assortment of active and passive devices need to be adequately provided with physical support, environmental protection, heat removal, electrical interconnections where specified, and electrical insulation where interconnections are not specified, all by a cost-effective means.

Packaging design is becoming more complex. Switching devices typical of digital electronics technology are continually increasing in both switching speed and in the number of devices per chip. Individual chips are being provided with greater numbers of connections that are in smaller individual chip package sizes. The competitive need to take maximum advantage of device density and speed has forced packaging designers to pay much more attention to the problems of electromagnetic wave-propagation phenomena associated with transmission of switching signals within the system. New design disciplines and design strategies are needed. This document is intended to help meet this need and this overview section will introduce in broad terms what is covered.

3.1 Decision Making Process Determine at the start of a project which packaging concerns need early introduction into the design process. Performance of older systems was limited by the devices available at the time and therefore packaging design could often be left for the end of the design activity. High performance systems are limited in speed by packaging, so if the project is concerned with speed, start by considering how to get the most out of the packaging today.

There are numerous design options to consider, and the designer will have to compromise between thermal, mechanical and electrical requirements of the package (see Figure 3-1). For a proposed system, a choice among types of electronic devices has to be made. This will have an influence on the kinds of packaging materials to be selected. It will become apparent that the design is a collection of compromises to get the best overall performance. Effort early in a program to evaluate many sets of options and their interactions is recommended.

The decision making cycle will consist of proposing a design with selection of devices, packaging materials, and interconnection schemes. The system preferably will be modeled and its deficiencies and limitations identified. This should result in some alterations in the design and the start

---

[1] www.ipc.org

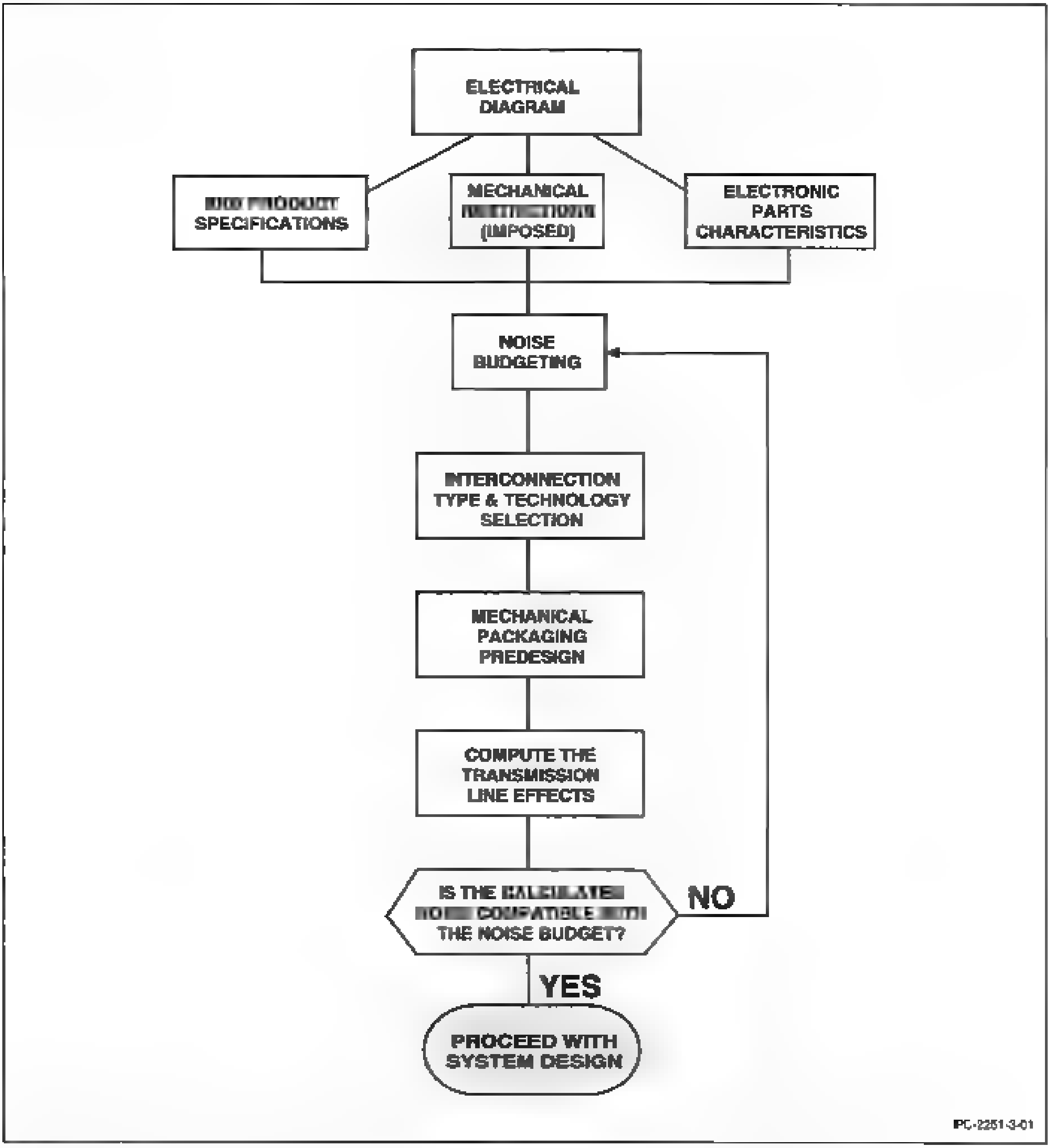

ELECTRICAL DIAGRAM
END PRODUCT SPECIFICATIONS
MECHANICAL RESTRICTIONS (IMPOSED)
ELECTRONIC PARTS CHARACTERISTICS
NOISE BUDGETING
INTERCONNECTION TYPE & TECHNOLOGY SELECTION
MECHANICAL PACKAGING PREDESIGN
COMPUTE THE TRANSMISSION LINE EFFECTS
IS THE CALCULATED NOISE COMPATIBLE WITH THE NOISE BUDGET?
NO
YES
PROCEED WITH SYSTEM DESIGN
IPC-2251-3-01

Figure 3-1 High-Speed Packaging Design Concept

of another modeling cycle. The process is repeated until further improvement is minimal. If the projected performance is far short of the target then the designer should consider attempting a different design approach.

These guidelines should be helpful to the designer in providing awareness of the options available and the principles needed in modeling. There is plenty of room for innovative advances in high-speed packaging.

3.2 Design Options Let us consider some of the options to be exercised by the designer, realizing that each selection interacts with the others. These options are listed in this section and are followed (see 3.3 and 3.4) by a list of corresponding requirements.

3.2.1 System Electrical/Mechanical Constraints What type of active switching devices will be used? Example options include TTL, Schottky TTL, CMOS, ECL, PECL, GTL, GTL+, and GaAs, each with its own set of power requirements, operating temperature range, density on a chip, input impedance, output impedance, signal threshold levels, noise sensitivity, response time and output pulse rise/fall time

How will the selected electronic devices be organized in the final assembly? Chip devices can be prepackaged and individually mounted on a large board or assembled into small boards or Multichip Modules, which will in turn be mounted onto large boards. Large systems will require several large board assemblies and there is yet another option of how this level of interconnection will be applied. Reflection noise and signal degradation will accompany transitions from one packaging level to the next. Organization will have an impact on manufacturability and repairability of the system.

What transmission line geometry on boards will be used for signal interconnections between devices? Options include coplanar coupled pairs, microstrip over a single ground plane, striplines between ground planes, orthogonal striplines sharing a common pair of ground planes, wire over ground plane, and wire between ground plane. For a given geometry, the selection of substrate thickness and conductor width will depend on the required characteristic impedance, and the relative permittivity (dielectric constant) and thickness of the substrate.

What interconnect schemes for signal transmission will be used? One could choose single connections from one device output to another device input. A single output could be connected to several inputs and the multiple connections could be accomplished either by branching or by continuing from one input to the next in daisy-chain fashion. The scheme will affect transmission time, noise, settling-time and signal pulse degradation.

3.2.2 Signal Integrity Design Constraints If the design of the system and circuit card assemblies are not controlled Signal Integrity cannot be achieved. These effects degrade noise margins, cause mis-operation and are indicated by overshoot, undershoot, nonmonotonic edges, signal line crosstalk, routed signal line induced skew, ground bounce, poor power quality, poor output drive due to loading effects, and EMI problems. These effects are usually controlled up front during the design phase, with component placement, PWB layer stack-up, and during the route.

3.2.2.1 Overshoot Signal line overshoot is caused by a reflection due to an impedance mismatch. Generally, the mismatch is caused when the source impedance of the driver is lower than the impedance of the trace conductor and destination load(s). During a transition, the rising or falling edge goes beyond the supply or ground reference voltages. For example: if a signal is transitioning from 0 Volts to 5 Volts, a reflection may "overshoot" the 5.0 Volt supply reference to a value of 6.5 Volts. While minor levels of overshoot may be acceptable, it degrades system noise margin budgets and may cause instability in ICs. Overshoot is controlled by proper signal line termination, logic family selection, driver slew rate or drive strength control, route topology, and managing the layer stack-up impedance.

3.2.2.2 Undershoot Signal line undershoot is caused by a reflection due to an impedance mismatch. Generally, undershoot is the result of an overshoot problem. It occurs after successive reflections causing a short additional pulse within the supply or ground rails after the original. For example: if a signal is transitioning from 4 Volts to 0 Volts, a successive reflection may "undershoot" the 0 Volt supply reference and generate a short additional pulse after the falling edge of 0.8 Volts. While minor levels of undershoot may be acceptable, the magnitude may exceed logic levels and cause an additional delayed logic state resulting in circuit mis-operation. Since undershoot is generally caused by overshoot, the same techniques used to control overshoot apply.

3.2.2.3 Nonmonotonic Edge A nonmonotonic edge is a "double transition" effect that occurs during a rising or falling edge, where two edges are generated (sometimes referred to as a double clock). For example during a rising edge, the signal rises and during the transition, falls for a short period of time then finishes the rising edge. Typically caused by poor route topology with a driver branching to more than one load of unmatched lengths of conductors. The short trace reflection and long trace reflection combine at the nearest receiver causing the effect. Where the nonmonotonicity occurs on the edge is important. If it occurs in the logic threshold region, it may cause a false logic condition resulting in mis-operation. Nonmonotonic edges are controlled by proper signal line termination, managing the route topology, and matching conductor lengths.

3.2.2.4 Signal Line Crosstalk Signal line crosstalk is discussed in 3.4.7 and 5.7 and 3.2 of Appendix B. Signal line crosstalk is managed by proper conductor placement and spacing.

3.2.2.5 Routed Signal Line Induced Skew Routed signal line induced skew is caused when additional unplanned delay or skew is introduced in the route of signal conductors. For example: A clock or data strobe is routed too long or too short for a data latch and the data is not stable (still settling) before the qualifying clock or strobe is presented. Incorrect data may be latched causing an error. Routed signal Line skew is managed by directing the router to match the lengths of signals in a group and matching loading delay. Critical timing lines should be identified and skew predetermined (route path and route length) before the

PWB is routed. Most layout tools are able to route to conductor length or delay matching rules to a predetermined tolerance. Some skew is acceptable and the amount is constrained by clock rate, set-up and hold times, edge rate, route layer definition, routing space, and crosstalk management.

3.2.2.6 Ground Bounce Ground Bounce is caused by a combination of problems. Ground Bounce is the effect when multiple outputs simultaneously switch from one state to another, which causes another "quiet" (non-switched) input or output to follow (bounce), the edges of the driven outputs. Most integrated circuits have inductance associated with bond wires (or carrier traces in high density IC interconnects) for inputs, outputs, power, and grounds. At high switching speeds, the inductive reactance may become significant particularly on the power and ground interconnects; this effect is a difference of voltage drop between the die pad and the package-pin pad or lead frame. When wide high-speed busses simultaneously switch from high to low or low to high, large amounts of instantaneous current is required to drive the bus load. The current must be supplied by the power and ground interconnects (bond wires or carrier interconnect). The resulting dI/dT required by the driven bus lines across the interconnect creates a voltage drop across the interconnect. This creates localized voltage shifts on the IC die, which allows a quiet line in that localized area to bounce. The amplitude of the bounce varies with the number of simultaneously switching outputs and the inductance of the IC power interconnects. Many vendors have reduced susceptibility to ground bounce by using multiple power and ground wires or interconnect (paralleled wires reduce inductance similar to resistors in parallel), or use shorter wires or interconnect (shorter length reduces inductance), or use the flip chip techniques instead of wire bonding (shorter length, controlled impedance, ground plane referenced results in less inductance). Another problem that aggravates ground bounce is bus loading. Generally, wide busses go to many bus elements (processors, cache ram, ram, memory controllers, etc.). Each I/O pin and its associated interconnect (trace capacitance) between each I/O is a capacitive load. The resultant capacitive load of the switched outputs is impressed on the driving IC power and ground bond wires or carrier interconnect. Reducing this load may reduce ground bounce. Sometimes, series resistors on the bus elements help limit the current but present other problems with component count, rise / fall time, and timing margins. Proper component placement (even distribution of routing stubs from the bus) and short interconnect helps reduce the capacitive loading, thereby reducing the risk of ground bounce. The power and ground plane inductance being too high may aggravate ground bounce. If the power or ground planes have too many localized via clearances, its inductance may be too high. This creates a poor source of power to the devices driving wide busses. The power and ground interconnects (vias or traces) should provide a low inductive source to ICs.

3.2.2.7 Poor Power Quality Poor power quality is generally caused by a lack of power decoupling, circuit isolation, and poor power regulation. Poor power quality degrades noise margins, is aggravated by environmental changes, causes timing problems, degrades edge rates, and is difficult to locate. Power decoupling and circuit isolation are covered in 5.1.4. Power regulation is covered in 5.1.

3.2.2.8 Poor Output Drive Poor output drive is caused by a device's output impedance being much higher than the load impedance. It is generally characterized by severely rounded off edges or poor noisy edges on the waveform. It causes poor timing margins due to the longer transitioning edges consuming a larger than anticipated percentage of the duty cycle. Poor drive erodes set-up and hold times. Careful attention must be paid to impedance matching, PWB layer stack-up, loaded line capacitance, stub distribution (see 5.6.3 through 5.6.6), minimizing trace lengths, and power quality.

3.2.2.9 EMI Problems EMI problems are covered in 5.11.1 through 5.11.3.7.

3.2.3 System Electrical/Mechanical Requirements The decision on the number of signal layers in multilayer boards or discrete wiring boards to be used will be influenced by the density of interconnections within the board. There will be a compromise on the degree of isolation of one interconnection from another versus the need to get a large number of interconnections in a given board area.

Determine the degree of crosstalk or coupling between signal lines that can be tolerated. This can have a major effect on acceptable interconnection densities.

Relative permittivity (ε_r) influences board substrate selection. While a low ε_r value means faster signal propagation it also increases the conductor width needed at a given substrate thickness for a given characteristic impedance, thus reducing room for conductors.

Power requirements of the devices will also need to be met. Often the choice is made to provide power planes in circuit boards that serve the dual roles of ground plane for signal conductors and power supply for the electronic devices. An alternative is to provide a power bus system to the array of devices on the board.

3.3 Mechanical Requirements The mechanical requirements listed within this section is given to help the designer maintain the integrity and performance of electrical interconnections among electronic devices in the system.

3.3.1 Circuit Board Circuit boards are required to provide mechanical support and interconnection of components mounted on them. Space constraints, number and complexity of interconnections, thermal management, power distribution, and cost of manufacture are some factors to be considered when determining requirements of how many layers to use, the thickness of dielectric layers, the composition and thickness of ground/power plane layers, the dielectric composition and the overall length, width, and thickness of the board.

3.3.2 Hybrid This term is often used to refer to assemblies of thin/thick film chip devices mounted directly on thin/thick film ceramic interconnection boards to form a multichip module. Other technologies using polymeric substrates in place of the thin/thick film ceramic could also be used to build multichip modules. Hybrid boards and multichip modules are usually required to provide protection of sensitive chip components from adverse effects of any environmental or operating conditions that may be encountered in service. They also must be able to withstand thermal and mechanical shock during manufacturing and assembly as well as in service.

3.3.3 Component Packaging Unless chip devices are packaged in multichip modules or hybrid subassemblies they are usually prepackaged individually. The component package can be polymeric or ceramic depending on the degree of atmospheric protection required. The package is required to provide protection to the chip and electrical connections from the chip to the board on which it will be mounted. The package also provides a means for connecting to the chip for automated testing of the package prior to its being used in a board assembly.

The electrical connections to the board can be of a variety of configurations ranging from pins that will insert into plated through holes provided in the board, as in dual in-line package, to a series of metallized regions along the edge or arrayed over the base of a surface mount device. What type of connection is selected will depend on, among other things, the requirements for electrical performance of the connections.

Requirements for component packaging will be dependent on many factors including space available, economics, electrical performance requirements, reliability, life expectancy, and thermal conditions.

3.3.4 Thermal Management The system must withstand thermal cycling and temperature differences during service. Temperature differences arise, especially in startup, between packaged electronic devices and the interconnecting board. This temperature difference will cause mechanical strain between the packaged devices and the board because of their different coefficients of thermal expansion. The greater the difference in the coefficient of thermal expansion (CTE) of the devices and the boards, the greater will be the mechanical strain.

The packaging materials must handle the heat generated by operating the system. Mechanical properties sufficient to provide mechanical integrity of the system must not change at the elevated temperatures expected to be encountered during system operation. Packaging must provide for removal of excess heat to keep the temperature below the point where impairment of electronic performance would [redacted]

3.3.5 Component Mounting The component must be provided in a physical format that is convenient to attach to the circuit board. Mechanical requirements imposed on the board by a component include the feature tolerances required for attaching the component to the board and the susceptibility to damage during attachment of the component. Some device packaging categories include:

a. COB mount device

b. TAB mount device

c. Single chip package (DIP, PLCC)

d. Multichip package

3.4 Electrical Considerations Electromagnetic wave propagation theory must be considered in evaluating the performance of interconnecting conductors and their substrates. High-speed devices are characterized by the fast rise time of the electrical pulses. The pulse waveform may be represented using the Fourier transform as the series of sinusoidal signals with certain phase and amplitude relationships. As the rise time of the pulse decreases, the frequency of the important components increases.

3.4.1 Power Distribution For high-speed devices, switching activity is accompanied by equally high-speed demands for changes in electrical current from the power supply. If several devices are demanding current changes at or near the same instant, the power distribution system is required to meet these demands while simultaneously maintaining voltage within specified limits to all devices being supplied. Meeting this requirement demands low inductance connections to devices, with high capacitance among various voltage levels in the distribution system.

3.4.2 Permittivity The relative permittivity (ε_r) of the dielectric substrate of an interconnecting device, whether it be a printed board, discrete board and a multichip module, or a chip package, will affect electrical performance of the interconnection on or embedded in it. An assumed ε_r is used in the design of the interconnection to meet the impedance, capacitance and propagation time requirements as will be discussed later. The tolerances of these requirements, along with manufacturing tolerances on conductor dimensions, impose a tolerance requirement on ε_r if the system is to perform as designed. Since ε_r of many substrate materials varies with composition, frequency, and environmental conditions, these variations also impact the allowable tolerances on ε_r.

The permittivity that actually affects transmission line electromagnetic wave propagation characteristics is what is called the effective permittivity, or $\varepsilon_{r,eff}$. The effective permittivity is affected by the geometry of the transmission line and by the dielectrics of and near the transmission line that is influenced by electromagnetic energy from the propagating wave or pulse. For a given transmission line geometry, propagation time and capacitance will vary directly by the square root of $\varepsilon_{r,eff}$. Impedance will vary inversely as the square root of $\varepsilon_{r,eff}$.

There are trade-offs in the selection of high or low $\varepsilon_{r,eff}$ values for the substrate that will be discussed later.

3.4.3 Capacitive Versus Transmission Line Environment For an interconnection from one device to another, the connecting line can be treated either as a transmission line or a capacitive line. For transmission lines, the design concept is to provide a known characteristic impedance that is terminated at the destination with a matching impedance to minimize reflections that result from fast rise time pulses. For a capacitive line, the concept is that of a line whose stored charge requires a certain amount of current flow to result in a change in the voltage that is present at the destination. The critical design parameters and requirements will depend on which concept is appropriate.

3.4.4 Propagation Time In high-speed systems, it is not unusual for the clock cycle time to be shorter than the propagation time for a signal from one device to another, especially where a signal might originate on one board and be received on a device on another board. For the system to perform correctly at high-speeds, a well-controlled propagation time is required and in some cases adjustments in the propagation time for certain signal paths (lines) may be required.

3.4.5 Characteristic Impedance The Characteristic Impedance typically used will range from 50 to 70 Ohms. This range of characteristic impedance is often used because lower impedance values cause excessive crosstalk between nearby signal lines and power consumption by impedance-matched electronic devices. Higher impedance provide lower crosstalk values for a given signal amplitude but produce circuits with greater EMI/ESD susceptibility, and greater EMI radiated emissions. Typical signal paths will have a characteristic impedance of 50 Ω for most printed wiring boards. Examples where 50 Ω is not used are: PCI, 100 Ω but is dependent on signal path length and load impedances (32 Ω is the minimum load impedance); Compact PCI, 65 Ω; RS-422/RS-485/LVDS differential traces, 50 Ω to 75 Ω for signal-line-to-ground impedance and 100 Ω to 120 Ω for signal-line-to-signal-line impedance; analog, 25 Ω to 100 Ω; and radio frequency, 50 Ω, 75 Ω, and 100 Ω, 75 Ω characteristic for RS-170 and RS-343 video traces. The impedance selected may be higher than 50 Ohms for large bus structures with multiple terminations to reduce driver loading and Ground Bounce. The characteristic impedance of a lossless uniform transmission line is equal to the square root of the ratio of inductance per unit length to capacitance per unit length. The impedance of a transmission line can be mathematically modeled as a complex function of several parameters.

a. Conductor width/diameter-impedance decreases with increasing signal line width or diameter.

b. Type of transmission line-Microstrip, Embedded Microstrip, Centered Stripline, Dual Asymmetrical Stripline, Edge Coupled Differential Pairs, Broadside Differential Pairs, and Coplanar (see IPC-2141). With equal ε_r, spacing and conductor width, impedance ranking will be, from highest to lowest: Differential Pairs, Coplanar, Microstrip, Embedded Microstrip, Dual Asymmetrical Stripline, and Centered Stripline. Refer to Figure 5-8.

c. ε_r of dielectric-impedance decreases with increasing values of ε_r

d. Spacing between signal and ground-impedance decreases for decreasing spacing.

e. Proximity to other conductors-impedance decreases as distance increases.

3.4.6 Signal Loading Effects When a signal line terminates into several electrical loads and if the power supply is not an ideal voltage source (which is usually the case), the issue of signal loading must be considered.

First, consider loads connected along the length of the signal line. If the impedance of the load is low or a near match to the characteristic impedance of the line, there will be a decrease in signal amplitude as each successive load in the signal path is encountered. High-impedance loads relative to the line will result in less decrease in amplitude. A matched load at the end signal line is needed to prevent a reflection that could affect circuit function. If the distance between loads along the signal line is approximately equal to or longer than the wavelength of the highest frequency component of the signal, the signal propagation along the transmission line must be considered when calculating loading effects. On the other hand, if the spacing between electrical loads is much less than a wavelength, then for practical purposes the loads appear to be connected at a common location or node. Consequently, the node will have low impedance and the signal amplitude to the loads will be diminished. The impedance at this node can be approximated using lumped-element analysis.

3.4.7 Crosstalk In general, an interconnecting board is populated as densely as possible with devices and conductors to minimize the size of the system and reduce propagation time along the signal lines. The result is that conductors must be placed close to each other and usually the designer must resort to multilayer boards or discrete wiring boards to accommodate the high interconnect density and the crossover situations in the wiring plan.

Crosstalk is the transfer of electromagnetic energy from a signal on an aggressor (source or active) line to a victim (quiet or inactive) line. The magnitude of the transferred (coupled) signal decreases with shorter adjacent line segments, wider line separations, lower line impedance, and longer pulse rise and fall times (transition durations).

A victim line may run parallel to several other lines for short distances. If a certain combination and timing of pulses on the other lines occurs, it may induce a spurious signal on the victim line. Thus, there are requirements that the crosstalk between lines be kept below some level that could cause a noise margin degradation resulting in malfunction of the system.

3.4.8 Signal Attenuation High-speed systems have devices that generate fast rise and/or fall time pulses and the devices may respond ambiguously to pulses exceeding a certain maximum rise time. This is best explained by considering the Fourier transform of a signal. The Fourier transform decomposes the signal into a series of harmonically related frequency components. This is best explained in terms of the model of a pulse as a sum of even and odd harmonic signals, where the harmonics are of greater frequency than the fundamental frequency. The high frequency components of the pulse attenuate more rapidly than lower frequency components. This is due to the skin effect in the conductor as well as the dissipation effect in the dielectric. Furthermore, for thin copper, the pretreatment may raise the copper resistance, which will increase skin effect losses. The skin effect losses may also depend on the finish of the copper surface.

The resistance of the copper may reduce the steady state voltage levels below the levels needed for adequate noise immunity. This is especially true of ECL circuits where a voltage divider is formed by the terminating resistor and the line resistance.

The DC resistance of a line can be calculated using the copper resistivity and the geometries of the line. The effects of surface finish (skin effects) may have to be determined experimentally. The smooth surface of a drawn wire used in discrete wiring boards has lower skin effect losses and other advantages over etched conductors.

4 MECHANICAL CONSIDERATIONS

In addition to meeting the predicted performance criteria, circuit board designs must be manufacturable if the system is ever to become a reality. Performance versus cost also factors into the choice of the optimum system design. Yield at manufacture and end product reliability may be, at times, even greater contributors to cost than the obvious costs of raw materials and fabrication. For this reason, the designer should be familiar with the material options available, their properties, capabilities, and tolerances and have a reasonably good understanding of process capabilities and tolerances that may impact not only performance, but also manufacturing yield and reliability.

The development of a close working relationship with the manufacturing engineering group of the captive or vendor board fabrication facility is highly useful to avoid excessive prototype iterations which are both costly, and time consuming. Designing "based on what worked before" is certainly valid but may be limiting at times if full advantage of advances in both materials and fabrication is to be taken. Therefore, the development of a relationship with in-house advanced materials and manufacturing groups as well as outside industry sources is advisable.

The following is intended to serve as a cursory overview of some of the interactions between raw materials, performance, and manufacturing capabilities. This summary should by no means be considered exhaustive of the technologies available for the production of circuit boards.

[illegible]

4.1.1 Substrate Materials Laminates and bonding material and their properties are detailed in IPC-4103.

4.1.1.1 Resin Systems The resin systems used for circuit board laminates are classified into two basic categories: thermosetting and thermoplastic. Thermosetting resins are cross-linked matrices of smaller, polymeric units. The polar nature of materials generally contributes to higher relative permittivity, loss tangent (dissipation factor) and water absorption. The cross-linked structure of the thermosets generally provides better dimensional and thermal expansion characteristics than thermo plastics. Water absorption becomes an issue because its relative permittivity is so high (approximately 75) compared to these resin systems. Therefore, relatively small changes in humidity in the environment may drastically impact performance (i.e., capacitance and Z_0) and necessitate strict environmental controls. Likewise, each resin system has a characteristic response of relative permittivity and loss tangent to temperature and operating frequency.

4.1.1.2 Reinforcements, Supports, and Fillers Although some of the available materials are comprised of resin only, routinely various reinforcements, supports, and/or fillers are incorporated with the various resin systems to enhance the physical or electrical properties of the composite laminate. A typical example is the incorporation of woven

E-glass into a resin matrix to enhance dimensional stability and reduce the X-Y coefficient of thermal expansion (CTE_{XY}), which may be unacceptable or undesirable in the unsupported resin. Fillers may be added to modify the relative permittivity and/or to exclude resin and thereby reduce the overall CTE in X, Y, and Z dimensions.

The thicknesses of woven glass reinforced materials are typically even multiples of the reinforcement thickness plus resin.

4.1.1.3 Claddings Copper is by far the most common cladding material around which most circuit board processes have been designed. Copper foils are sold by weight, with 1/2 (153), 1 (305), and 2 (610) oz/ft^2 (gm/m^2) being common. These weights roughly translate to 0.018 mm, 0.035 mm, and 0.07 mm [0.0007 in, 0.0014 in, and 0.0028 in] in thickness respectively. Thinner foils are available.

For high-speed circuitry it may become necessary to provide special cladding material:

- With reduced (inner) surface roughness (≤2 µm [78.7 µin]) in order to minimize line resistance.
- Permitting advanced interconnection techniques (e.g., ultrasonic bonding).

Copper foils are available in rolled annealed or electrodeposited forms. Other properties of copper foils relate to their ductility and elongation characteristics, which may impact through-hole reliability. For more information on foils, consult IPC-4562. Untreated copper foils shall have the following maximum resistivity at 20 °C [68 °F].

For deposited foil:

Weight Designator	
E	0.181 ohm-grams/meter^2
Q	0.171 ohm-grams/meter^2
T	0.170 ohm-grams/meter^2
H	0.166 ohm-grams/meter^2
M	0.164 ohm-grams/meter^2
1 oz. and over (305 gr/m^2)	0.162 ohm-grams/meter^2

For wrought foil (all weights):

Type 5, 8	0.158 ohm-grams/meter^2
Type 6	0.153-0.157 ohm-grams/meter^2 according to temper
Type 7	0.152 ohm-grams/meter^2

4.1.1.4 Discrete Wiring The wire resistivity of insulated wires for high-speed circuitry utilizing discrete wiring boards is shown in Table 4-1.

Table 4-1 Wire Resistivity

Diameter	AWG	Resistivity @ 20 °C [68 °F]
0.064 mm [0.0025 in]	42	1.80 ohms/ft
0.1 mm [0.004 in]	38	0.648 ohms/ft
0.16 mm [0.0063 in]	34	0.261 ohms/ft

4.1.1.5 Prepregs, Bonding Layers and Adhesives Various thermosetting and thermoplastic materials are available for laminating the multilayer package. Prepregs are woven glass supported resins in their B-stage or partially cured state. They are used to create the dielectric spacing between layers and are cured or cross-linked in the lamination process. Thermoplastic bonding layers may also be used for dielectric spacing and work by fusion bonding in lamination cycles exceeding their melting point. Thermoplastic bonding films and thermosetting adhesive films are thus unsupported materials used in configurations where the dielectric spacing is already provided by another material.

4.1.1.6 Material Tolerances Knowing the raw material tolerances from the outset will go a long way toward predicting the probability that a given design will perform within the desired specifications and form the basis for any sensitivity analysis. Impedance calculations are heavily impacted by thickness (dielectric spacing) and relative permittivity; therefore, these are of primary interest.

1. *Relative Permittivity* (ε_r) – The relative permittivity of the un-reinforced materials should be invariant as these are generally uniform, isotropic materials. The reinforced, supported, and filled materials are combinations of materials of different relative permittivity and will exhibit variations in this value unless the proportions of the combination are strictly controlled.
2. *Thickness* – Changes in the volume percent of resin will impact both thickness and relative permittivity. Thickness uniformity among materials will vary with the technology and the level of process control employed.

4.1.1.7 Material Impact on Board Fabrication/Assembly The specific details of circuit board manufacture are not discussed here. However, the effects of materials properties on manufacturing issues are listed as they impact design considerations. This list is not exhaustive.

1. *CTE_{XY}* – The expansion characteristics of the printed board under thermal load will impact the choice of components, the style of leads, and the method of mounting to minimize CTE mismatches that may ultimately reduce joint reliability. The reverse is also true. If the choice of component package and lead has already been made, then the material choice follows. In other cases, other materials may be incorporated into the package to further constrain movement in the X-Y plane further

reducing any CTE mismatch. Various thermal management schemes may also provide some relief in this regard.

2. ***CTE_z*** – Thermal expansion in the z-axis may impact through-hole (PTH) reliability in fabrication, assembly and in service. Advanced techniques or controls may be required to utilize high z-axis expansion materials. The number of layers or the overall thickness of the package may have to be limited or in some cases may preclude the use of PTHs altogether. Use of discrete wiring for replacing multiple etched signal layers can significantly reduce board thickness and eliminate z-axis expansion concerns.
3. ***Young's Modulus*** – The ratio of unit stress to unit strain.
4. ***Poisons Ratio*** – The ratio of lateral strain to longitudinal strain.
5. ***Dimensional Stability*** – Dimensional changes in the material impact layer-to-layer registration. Advanced techniques or controls may be required to utilize less stable materials.
6. ***Thermal Properties T_g*** – The glass transition temperature T_g of the material will dictate the thermal processes employed either in fabrication or component attachment.
7. ***Chemical and Solvent Resistance*** – These properties will dictate chemistries that can and cannot be used for processing and cleaning.
8. ***Machinability*** – The relative ease with which a material can be drilled, punched, and routed will impact the cost of fabrication.

4.1.1.8 Circuit Board Fabrication and Tolerances A general understanding of the capabilities of board fabrication technologies and the realistic and achievable tolerances is critical to the successful implementation of designs. Areas of particular interest are:

a. ***Hole Location and Diameter*** – impacted by drills, material, dimensional stability, drilling practices, and plating.

b. ***Conductor Width and Spacing*** – impacted by artwork, imaging, copper foil thickness, etching and plating. The PWB conductor is determined by wire size selection, and can be spaced on a variable XY grid or on the 45-degree diagonal.

c. ***Conductor Geometry*** – impacted by imaging technique, cleaning, etching and plating. The DWB inherent wire uniformity is not affected by subsequent fabrication processing.

d. ***Dielectric Spacing*** – impacted by choice of prepreg or bonding layer or film and lamination conditions.

Note: Prepreg thickness (and therefore permittivity) may vary with pressing conditions. For calculation purposes, the designer should consider the effective permittivity and thickness of a prepreg after the lamination cycle and account for any permittivity mismatches that may exist between the prepreg and other layers.

4.2 Component Packaging

4.2.1 Device The component package must be considered when selecting high-speed design rules and determining properties. The device package will establish thermal and electrical guidelines. Lead length is the predominate factor for passive components. The leads provide additional inductance and capacitance, which will affect propagation speed and switching transients. To minimize these effects the leads should be trimmed as short as possible or removed. Surface Mount Device packaging can provide leadless devices, which can be directly mounted to the interconnecting substrate. It is important to note that component data sheets often do not provide parasitic values for high-speed noise and propagation speed calculations.

Active devices, such as integrated circuits, are often offered in several package styles that provide various electrical and thermal performances. In general use, DIP packages have been the predominate package in either plastic or ceramic. These typically are the largest packages and provide the worst high-speed operating environment. The next best package style is the Surface Mount Package. These are offered in either Chip Carrier or Small Outline IC packages. These typically will reduce the lead capacitance and inductance. SM packages can easily be automatically assembled and handled. To obtain the optimum performance from the device, assuming operating conditions and reliability standards can be met, the die should be directly mounted to the substrate using either the Chip-on- Board (COB) or Tape Automated Bonding (TAB) approach. These offer the optimum approach since no additional capacitance or inductance is added with the exception of the bond wire (for COB) or copper conductor (for TAB).

4.2.2 Connectors Board to board connections are often the most troublesome high-speed connections because a continuous signal path is not possible due to mechanical constraints. There are two primary approaches to reduce the signal discontinuity.

The first approach assumes that the connector style is fixed, so the pin-out must be modified to provide a good signal path. Nondifferential signals reference between the active signal line and the closest voltage or ground reference plane.

Board to board connections are often troublesome because of mismatches in characteristic impedance. Nondifferential signal conductors rely on controlled geometries and nearby

AC reference planes (either DC voltage or ground planes) for impedance control. These geometries are interrupted in the connector.

Efforts to control signal and reference pin quantity and location in the connector should be made to control electrical performance.

To reduce the noise more reference pins must be added to reduce the distance and sharing problems. Generally a 3:1 signal to reference pin ratio is sufficient. The best ratio is 1:1, but may be too expensive, or consume too much real estate.

The second approach is to modify the connector. The intent is to minimize the discontinuity distance between boards. Either shortening the pin length, or adding reference ground plane within the connector can be used.

4.2.5 Cables High-speed cables must provide a good signal environment. There are three areas that must be considered; signal propagation speed, crosstalk, and induced noise.

Crosstalk can be minimized by several methods. The easiest is to put ground lines between the signal lines to isolate adjacency. A ground plane can be added which lowers the signal line impedance. The best method is to completely isolate signals using a coax line environment. This provides total isolation, but also is the least dense approach.

Putting a shield between the signal line and the radiating source can lower induced noise coupled onto the lines. Using the ground planes mentioned above, or providing an additional shield plane over the entire structure can accomplish this.

4.3 Thermal Considerations Electronic equipment processes information at the expense of electrical energy. The electrical energy fed to the machine is converted into other forms of energy and dissipated into the machine environment. There are two main ways of dissipating this energy.

- Electromagnetic Radiation
- Heat (Thermal Energy)

The electromagnetic radiation is generated because interconnections between two points on a board act as an unintentional antenna. The greater the area enclosed by the loop and the higher the frequency and the input current, the higher the level of energy radiated from the system. Even though the continuous increase of signal speed in equipment increases the amount of radiation, the quantity of energy lost in this way is negligible when compared with the quantity of energy converted to heat. Because industry regulations limit the amount of energy radiated from the system in the form of electromagnetic waves, this form of energy is generally captured by enclosures and eventually transformed into heat before it dissipates to the environment.

In order to understand the new aspects of the problem created by increasing the signal speed, one has to start by considering that with slower technologies the partitioning of the board is independent of the electrical signal characteristics. Under such conditions, the device positioning on the board and routing of the interconnect traces can be done keeping a few considerations in mind, such as thermal requirements. Under the high-speed conditions, the characteristics of the signal will practically dictate the positioning of the device, the routing of the interconnections, and the material to be used as well as the size and characteristics of the device package. All of these determinants will have very strong impact on the selection of the cooling option and the entire thermal design of the system.

4.3.1 System Level Impacts The increasing of the signal speed is necessary because it can increase the quantity of information that is processed per unit of time. As mentioned before, electronic equipment processes information at the expense of energy (electrical), which is absorbed from the source and lastly transformed into heat that must be removed from the system. For example, Figure 4-1 shows a schematic representation of flows of information, electrical energy and heat in a computer room environment.

With electronics becoming more powerful due to the use of high-speed technology, the energy required to operate the whole system of information processing and heat disposal is becoming a matter of great concern to both the manufacturer and customer alike. Translating this issue into thermal terminologies; "high-speed" often means more heat dissipation per unit volume. Ambient air generally is the ultimate heat sink, therefore it is expected that the temperature of this air will increase resulting in a "hotter" environment for any considered device. The possible solutions at the system level are:

- Increasing ventilation in order to reduce the air temperature by injection of cold air from outside.
- Use of heat exchangers (air to water or coolant) in order to evacuate the heat accumulated in the air in such a way as to reduce the ambient air temperature.
- Use of active mechanical systems for air conditioning.

Replace the air as a cooling agent with other fluids which have a higher specific heat capacity and are easier to circulate and refrigerate (such as water, freon and other organic fluids).

4.3.2 Board Level Impacts The effect of heat on high-speed signals can be immense. Electronic signals typically degrade as the temperature increases. Slower signal transition times result and they may become more sensitive to system electrical transients.

The success of any thermal management approach depends mainly on the ability of the designer to find a way to "spread" the concentrated heat over a larger area in order

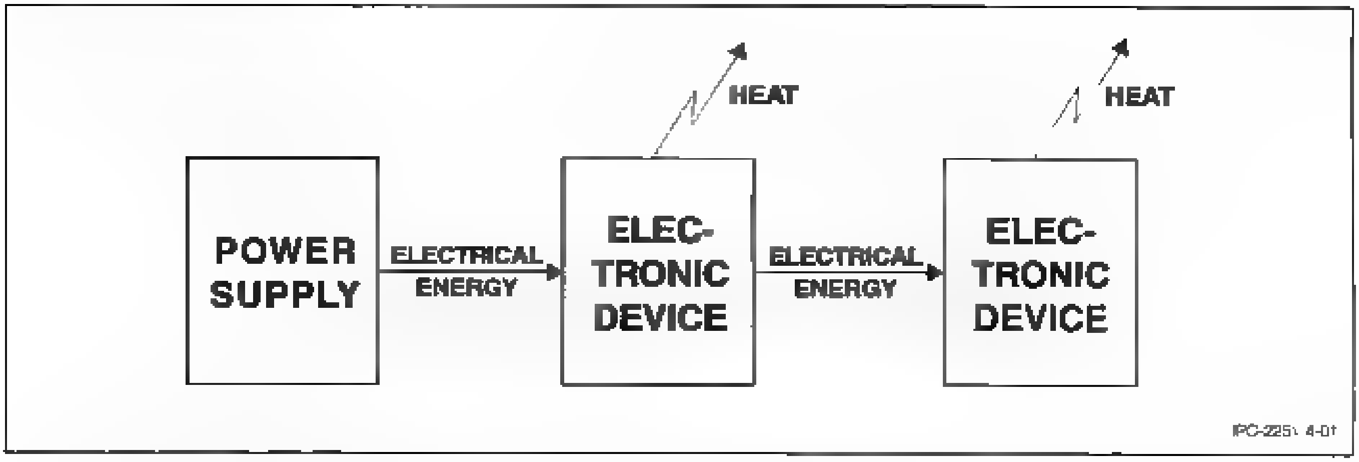


Figure 4-1 Schematic of Information, Electrical Power and Enthalpy (Heat) Flows

to reduce the peaks of the temperature field created by uneven power dissipation. This task is especially difficult today when we consider the properties of the materials involved in high-speed technology: materials with a low permittivity are needed, but these tend to have very poor thermal conductivity as well. For example, in order to spread the heat conducted by an active device, hybrid technology with a ceramic substrate is usually utilized. If the requirements for speed are very high, ceramic substrates may not be a viable option because they have a permittivity two to four times that of FR-4 glass epoxy. Possible solutions to confine this problem are:

- Better air flow management that ensures directing of the air to overheated areas.
- Conduction cooling and thermal spreaders (the heat is conducted to larger areas from which it can be removed).
- Immersion of the electronics in dielectric fluids.

Immersion cooling could be considered a very costly, efficient way of dealing with both high power dissipations as well as uneven dissipations of high concentrations in small volumes.

Beside the capability to spread heat rapidly into the entire volume of the enclosure these fluids can also act as cooling agents by absorbing the heat from the devices and transferring it either to another cooling loop or directly to the environment. The boiling temperature of the immersing fluid can be selected in such a way as to coincide with the maximum temperature admissible in the system. Phase changing of the fluid (boiling and condensation) could practically maintain the temperature of the electronics at a preset constant.

In order to understand the impact that high-speed technology has had on thermal design, one has to consider the multi-chip modules symbolized in Figure 4-2 by double circles. Joining together a certain number of semiconductor chips with controlled impedance transmission lines in order to achieve particular electrical performance creates high-speed multi-chip modules. However, grouping the devices close together in order to reduce interconnection distance may produce localized hot spots.

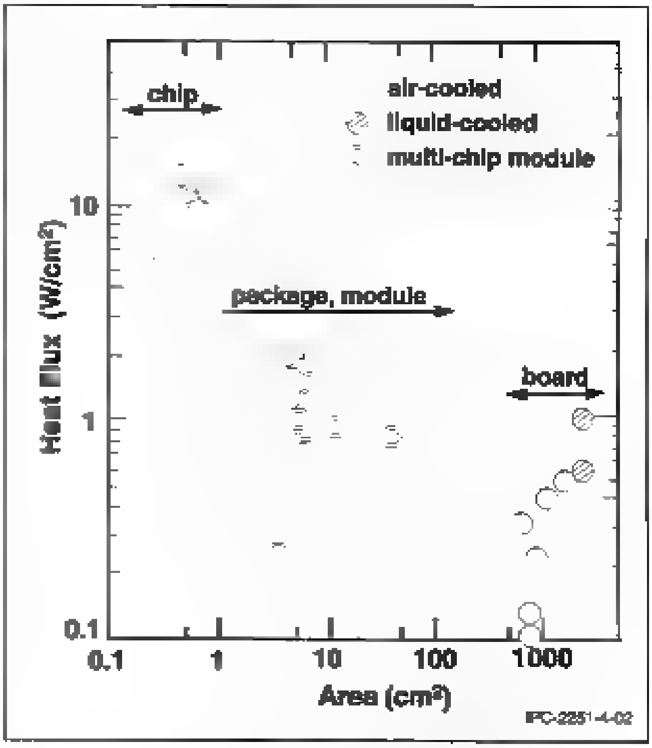


Figure 4-2 Heat Flux vs. Component Area

4.3.3 Device Level Impacts The component package has a direct impact on the performance of the device. At the same time the thermal characteristics of the device package are worsening almost linearly with the decrease of the device size. Generally, a way of improving the device package thermal performance is the use of ceramic materials for enclosures. As specified in the previous discussion ceramic materials have higher electrical permittivity that will negatively impact electrical performance of the package if very high-speed devices are involved. Low permittivity materials that improve the electrical performance tend to be very poor thermal conductors and also trap heat inside the semiconductor enclosure. Higher speed is usually associated with a temperature rise in the semiconductor itself and this presents an important challenge when high reliability of the product is required. Reliability decreases as temperature rises.

4.4 Component Placement Component placement is a critical factor in the design of high-speed systems. The effects of improper placement can be significant and include concerns in the following areas.

- Crosstalk Management
- Impedance Control
- Power Distribution
- Thermal Management
- System Cost

4.4.1 Crosstalk Management Typically, crosstalk is a concern when high-speed devices are used because of the high harmonic frequency content. Mixing logic families also causes concern because of the mixture of various voltage swings, noise margins and logic levels. An example would be mixing Schottky TTL and ECL logic families. The concern here is coupling from the TTL signals to the ECL conductors. Since TTL swings 3 volts and the ECL family has only a -100 mV DC noise margin significant undesired coupling can occur.

When copper planes are used to distribute logic levels, crosstalk (coupling) can also occur through the ground return path for these signals. This is called common mode impedance coupling. Essentially, a returning signal causes a ground potential rise due to the DC resistance of the plane. This problem can be very significant especially in analog circuitry when digital logic is present.

Several techniques can be used to control crosstalk in these environments.

a. Confine logic families geographically.

b. Restrict signal conductors for each logic family to those areas.

c. Provide separate return paths for each logic family.

d. Place components away from I/O connector in ascending order of speed (see Figure 4-3). Taking care to keep the high-speed signals away from the board edge. This will reduce EMI emission and improve EMI immunity.

e. Terminate controlled impedance conductors to reduce reflections that generate more noise.

f. Restrict conductor parallelism.

g. Specify and control conductor-to-conductor spacing.

h. Place components close together to minimize conductor lengths and parallelism.

i. Lower the relative permittivity.

j. Reduce the signal to ground separation.

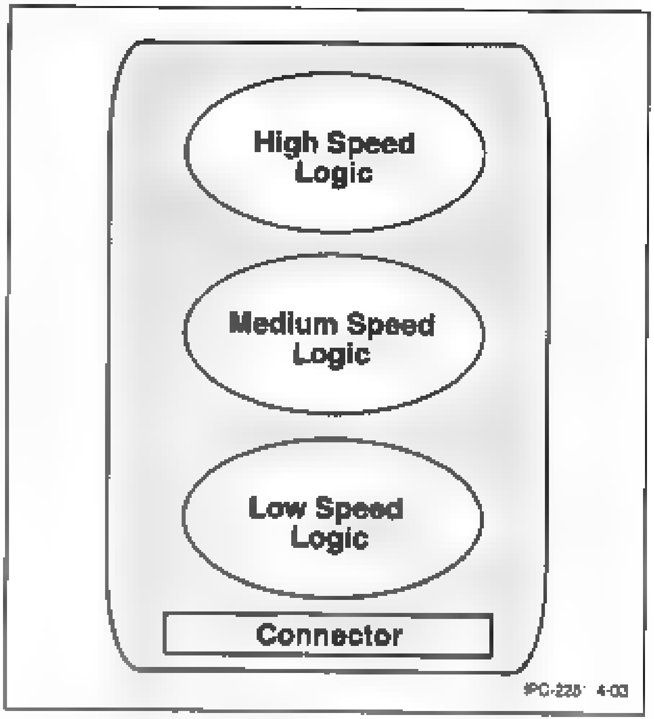


Figure 4-3 Component Placement Guideline

The impact on circuit board design due to these considerations will include:

a. Circuit board technology must now be capable of managing crosstalk.

b. Multiple power and ground planes required.

c. Added density due to the addition of terminations and tight placement.

d. Selective signal routing criteria.

These can greatly increase complexity and place limitations on the available circuit board technology.

4.4.2 Impedance Control In cases where high-speed signals are being transmitted, the signal conductors may need to be considered as transmission lines. This means, as a minimum, specifying the characteristic impedance of those lines. Since transmission lines should be terminated in their own impedance, a designer must provide for termination resistors.

Specifying a controlled impedance board and providing for termination resistors will add complexity to the design.

a. Termination resistors (one for each signal line) increase density and complexity.

b. Placement should be made so that each signal travels the shortest path from source (first point) to termination. Poor placement can result in very dense signal routing.

c. Circuit board technology must now be capable of controlling impedance.

d. Minimum component-to-component spacing may eliminate the need for controlled impedance lines but may greatly increase density.

4.4.3 Power Distribution Higher speed devices require the power supply to provide energy quickly. Figure 4-3 illustrates a typical board placement that shows the lowest speed logic near the connector and the highest speed logic away from the connector (This assumes the use of decoupling capacitors to provide the instantaneous power required for high speed devices.) Placement of these devices is not only dependent on performance requirements, but also on thermal requirements and capabilities.

4.4.4 Thermal Management As mentioned, high-speed devices can consume great amounts of power, and consequently dissipate much heat. In the placement of components, the following thermal management techniques should be considered.

a. When possible, "hot" components should be spaced apart as greatly as possible.

b. Convection Cooling-Components should be placed such that air flows parallel to component orientation.

c. Conduction Cooling usually involves the placement of a metal 'heat sink' or 'chill plate' on the surface or buried within the board. In these applications, placement must allow for sufficient metal surface area (i.e., usually requires greater component spacing).

4.4.5 System Cost Consideration should always be given to the cost of design and manufacturing. Generally, complexity adds density and cost. Cost does not necessarily just mean dollars. Cost can include lead times and reliability. Over-specifying a design "to be sure it will work" can significantly impact total cost.

Designing high-speed circuits is rarely a simple matter. There are many factors to take into consideration that usually act in direct opposition to one another.

Placing high-speed components closely together might reduce the need for transmission line parameters and reduce crosstalk problems, but may result in thermal management problems and increase the number of layers in a circuit board (due to increased density). Increasing the spacing will reduce the thermal problems but could add crosstalk and impedance restrictions. We can see that in high-speed design there are many considerations. It is the job of the circuit designer to understand the system specifications and weigh the alternatives to provide the simplest, cost effective, reliable solution for meeting those specifications.

5 ELECTRICAL CONSIDERATIONS

5.1 Power Distribution This section presents information used for calculating low and high frequency noise characteristics for system power distribution. Factors degrading power distribution may be grouped into two major categories; metallic losses and parasitic inductance in capacitors, IC lead frames, and planes. Spurious radiation loss is generally negligible.

The DC power distribution system encompasses the system from the output of the power supply to the input of each device. For systems with many cards and supplies, a simulation of the interaction of each component is desirable to verify and assist the design effort.

5.1.1 System DC Model The DC distribution model is comprised of lumped resistance for each element in the system. Figure 5-1 shows the interconnection and the major subsections of the model. This DC model analysis determines the DC voltage drop between the power supply and every integrated circuit location. The major elements in this model are described below.

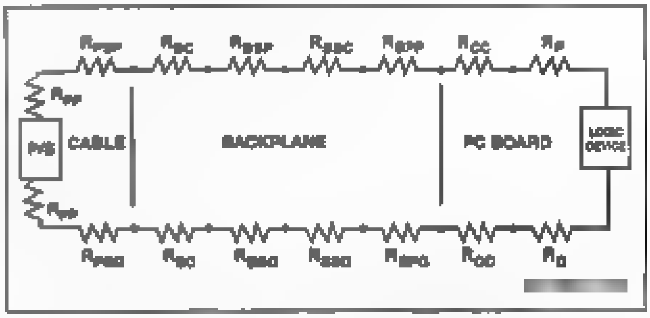


Figure 5-1 DC Distribution Model

5.1.1.1 Power Supply to Power Supply Cable Resistance (R_{PP}) R_{PP} is the contact resistance of the power supply cable to the power supply output. There is a contact resistance for each cable. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact. It is recommended to use a bolt, washer, etc., to keep the voltage drop less than 5 mV.

5.1.1.2 Power Supply Cable/Harness Resistance (R_{PSP}, R_{PSG}) This is the resistance due to the interconnection cable or harness from the power supply to the backplane or backplane power distribution busbar. The interconnection can take the form of a cable (circular or flat) or a busbar. R_{PSP} is the resistance of the positive voltage cable. R_{PSG} is the resistance of the power supply ground return cable. Typical resistance for various gauges of copper stranded, rope wound, medium hardness cables at 25 °C [77 °F] are listed in Table 5-1.

5.1.1.3 Power Supply to Busbar Connection Resistance (R_{BC}) This is the contact resistance of the power supply cables to the backplane busbar. There is a contact resistance for each cable. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact. It is recommended to use a bolt, washer, etc., to keep the resultant voltage drop less than 5 mV to10 mV

Table 5-1 Copper Wire Characteristics

Gauge	Number of Strands	Diameter in.	Area sq. in.	Resistance mΩ/ft.
2/0	19	0.419	0.1045	0.08224
1/0	19	0.373	0.0829	0.10370
1	19	0.332	0.0657	0.13080
2	7	0.292	0.0521	0.16490
3	7	0.260	0.0413	0.20790
4	7	0.232	0.0328	0.26220
5	7	0.206	0.0260	0.33060
6	7	0.184	0.0206	0.41690
7	7	0.164	0.0164	0.52570
8	7	0.146	0.0130	0.66290
9	7	0.130	0.0130	0.83590
10	7	0.116	0.0082	1.05400
12	7	0.092	0.0051	1.67600
14	7	0.073	0.0032	2.66500
16	7	0.058	0.0020	4.23700
18	7	0.046	0.0013	6.73800

5.1.1.4 Busbar Resistance (R_{BBP}, R_{BBG}) This is the resistance of the backplane power distribution busbars from the power supply cable contact to the backplane contact. R_{BBP} is the positive busbar resistance. A busbar is a metal strip that has a lower resistance than the backplane or circuit board. R_{BBG} is the ground return busbar resistance. For multiple backplane connections, this resistance will be modeled as a series of resistances between each backplane connection point. Cross-sectional resistances for copper (99% pure) at 25 °C [77 °F] are listed in Table 5-2.

Table 5-2 Copper Busbar Resistances/ft

Cross-Section Area (sq. in.)	Resistance (mΩ)
0.1662	0.050
0.1318	0.063
0.1045	0.080
0.0829	0.102
0.0657	0.128
0.0521	0.162
0.0413	0.204
0.0328	0.257
0.0260	0.324
0.0206	0.409
0.0164	0.515
0.0197	0.650
0.0103	0.820
0.0082	1.033
0.0065	1.300
0.0051	1.640

5.1.1.5 Busbar to Backplane Connection Resistance (R_{BBC}) This is the contact resistance of the backplane busbar to the backplane. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact.

5.1.1.6 Backplane Resistance (R_{BPP}, R_{BPG}) This is the plane resistance from the busbar contact to the circuit board (daughter card) connector. R_{BPP} is the positive voltage plane resistance. R_{BPG} is the ground return plane resistance. Since most power distribution systems have distributed daughter card contacts R_{BPP} and R_{BPG} will be the resistance between each contact point.

5.1.1.7 Backplane to Daughter Board Connector Resistance (R_{CC}) This is the backplane to daughter board connector pin and contact resistance. This resistance should be the value at the end of life. For a multiple backplane to daughter board interconnect scheme the resistance will be broken down into each contact. For lumped connector pin locations, the pin resistances can be paralleled. For two-piece connector systems R_{CC} is the total resistance for both connectors.

5.1.1.8 Daughter Board Resistance (R_P, R_G) This is the power plane or line resistance for the daughter board. R_P is the positive voltage plane resistance. R_G is the ground return plane resistance.

5.1.1.9 Paralleling of Power and Ground Conductors It is recommended that multiple cable conductors and/or connector pins be provided for power and ground connections. This accomplishes two major goals of power distribution and signal integrity. It reduces the resistance and inductance of the conductors by paralleling them. This is especially important in high-speed designs due to the instantaneous current demands placed on the interconnects. In addition, multiple pins offer long-term protection. As the mated connections age, oxidation occurs and their resistance increases. Multiple pins help keep the resistance low to avoid runaway heating degradation. Occasionally, a pin is mechanically damaged or overheated during its life by multiple insertions or hot plugging, providing multiple pins reduces the resulting failure and/or intermittent problems.

5.1.2 Power Plane Impedance The power distribution planes utilized in backplanes and daughter boards do not have zero impedance. Likewise the power supply does not have a zero source resistance. A circuit diagram of a multilayer power distribution network is shown in Figure 5-2.

The power supply is represented by a voltage source VS, R_{SP}, and R_{SG} (see Figure 5-2). The distribution impedances are broken out as backplane and daughter board sheet inductances, resistances, and plane-plane capacitance.

5.1.2.1 AC Impedance The power distribution AC impedance is subdivided into three components as shown in Figure 5-3. The first is the switching transient impedance

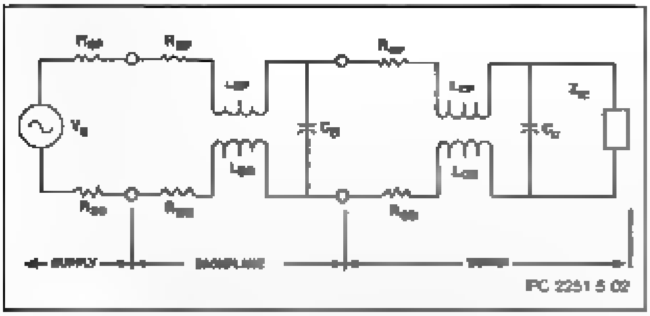


Figure 5-2 DC Power Distribution System (Without Remote Sensing)

(Z_{SW}). This impedance corresponds to the interconnect between the plane capacitance and the component. Using internal power planes that are very closely spaced can increase this capacitance reducing the effective impedance.

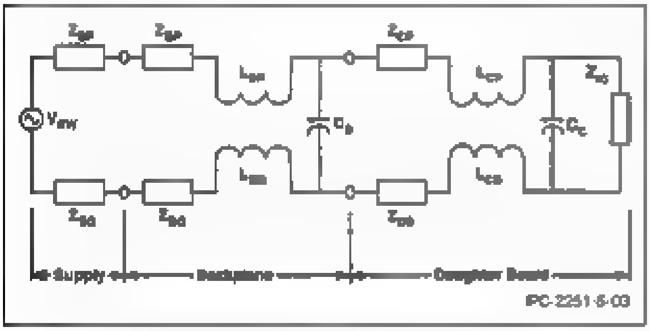


Figure 5-3 Decoupling Impedance Modeling - Power Supply

The second component is the impedance due to the bulk capacitor charging the IC decoupling capacitors (Z_{BC}). The current in this impedance is lower frequency and higher amplitude than the current in the first component. The voltage drop due to the lower impedance because of the lower frequency involved will be less than the above case.

The bulk decoupling capacitance refresh component (Z_{RC}) is the final element of the circuit board decoupling impedance. This current is responsible for recharging the bulk capacitors. It is supplied from the power supply and will usually have the lowest frequency component of the current.

Each of the board impedance components will be modeled as a transmission line plane-over-plane network. This closely models the worst-case configuration because of the regular layout of the printed circuit boards. A brief explanation follows.

The general impedance equation for parallel planes is as follows (reference Figure 5-3):

$$Z_p = \sqrt{R_p^2 + (L_p - C_p)^2} \qquad [0.1]$$

where: $L_p = \sqrt{2\pi f L}$
where L is plane inductance
R_p = Plane Resistance

$$C_p = \frac{1}{2\pi f C}$$

where C is the plane capacitance

5.1.2.2 DC Resistance The static voltage drop between any two points on a copper plane is determined by multiplying the maximum load current by the plane sheet resistance, R_T.

$$R_T = \frac{679}{T_p\ \mu\Omega/\text{square}} \qquad [0.2]$$

where: T_p = thickness of plane (mils)

A model analysis is used to determine R_T between each integrated circuit location. A computer program can be utilized to simplify the calculations. Each device is modeled as a point load and each connector pin is treated as a point source.

5.1.3 Integrated Circuit Decoupling A packaged device must provide sufficient current for its circuitry to operate. This includes high peak current requirements during output switching. The circuit board power system must provide this current without lowering the input supply voltage below its required minimum level.

When the power supply is too far away or the stored energy in the board is insufficient, capacitors are placed near the devices, connected between the power and ground planes to provide this current. In a sense, these capacitors provide the charge current to the device instead of the power planes. The power plane creates a capacitor that can also provide a small amount of high frequency current. These planes should be spaced very close to maximize their capacitance. When they discharge their current into the device they quickly recharge from energy stored in slower discharging capacitors and power supplies in time for the next required discharge.

5.1.3.1 Decoupling Model Figure 5-4 presents a device-decoupling model. Shown are the decoupling capacitor, power planes, signal load, and device models. The device decoupling system is composed of several elements. Every element can be modeled as a network of resistors, capacitors, and inductors. Figure 5-4 illustrates the interconnection of the following decoupling system components:

Decoupling Capacitor - (C_D)
Device Power Lead - (R_P, L_P)
Device Ground Lead - (R_G, L_G)
Transmission Line Load - ($Z_O + Z_{LOAD}$)
Destination Load - (Z_L includes C_{LOAD}, R_L, L_L)
Power Plane - (C_D, C_{Plane})
Power and Ground input vias - ($L_{P\text{-}In}$, $L_{G\text{-}In}$)
Trace and via inductance ($L_{V\text{-}Trace}$)

Note: Some parasitics not shown.

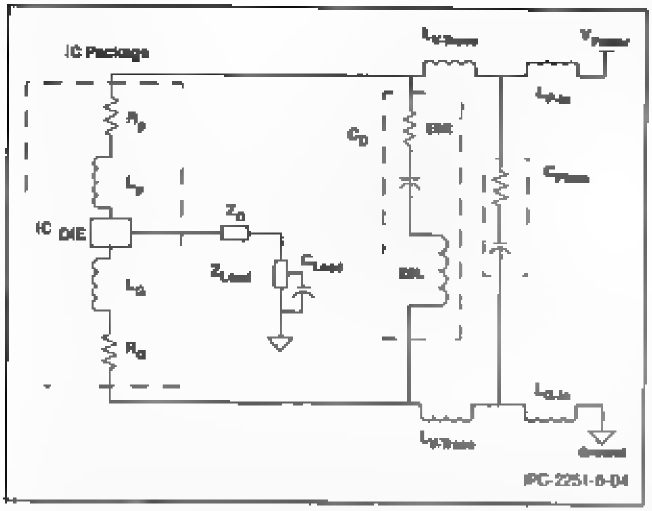


Figure 5-4 Device Decoupling Model

5.1.3.2 Switching Current Frequency Content An integrated circuit has two power supply current components: steady-state bias and output drive. Component data sheets, SPICE models, IBIS models and other proprietary models provide these current specifications.

The steady-state bias current is listed over the full temperature and supply voltage specifications. On large devices, such as microprocessors and memories, an average value is provided for power supply size estimation.

In CMOS devices the frequency dependent output drive current is typically not specified and must be calculated. This is especially true of large programmable devices. Some large programmable devices have multiple supply voltages. Some have one supply voltage for the logic core and another voltage for the I/O drivers. Since these currents are almost always dependent on the operating frequency and/or loaded drive, the vendor's calculations should be used. Most device manufacturers supply calculation approximations for frequency dependent power dissipation on their web sites. Because the signal loads and the device outputs are nonlinear, the current is typically best characterized by a time dependent current waveform.

The frequency response required by the decoupling capacitor system (actually, a network), may be predicted by transforming the time domain waveforms into their frequency components (spectra). The frequency response for the power system should be modeled based on expected activity in locations on the board. This will be generally be dominated by device risen times, not just the primary clock frequency. Many parameters must be considered when designing the Power Distribution System (PDS) of a board or system. The PDS should be considered as individual partitions of circuitry that may include multi-sourced voltage supplies. For example, a modern CPU device will have high frequency core voltage requirements and somewhat lower frequency I/O requirements. Exceptions to this may be with serial I/O schemes or Phase Lock Loop (PLLs) that may be built into the CPU device, which may have very high frequency requirements. Memory devices will have high frequency current requirements that are often at a different voltage source than the CPU core. I/O devices may have multiple frequency and voltage requirements from simple status monitoring/controlling (very low frequency) to high-speed serial and parallel data rates (very high frequency).

5.1.3.3 Inherent Plane Electrical Model 5.1.2.1 presented the parallel plane impedance of a two plane power distribution system. The power distribution model can be partitioned on a per device basis. In the per device model, the plane inductances (L_P, L_G), parallel-plane capacitance (C_P), parallel-plane impedance (Z_P), and plane resistance (R_P) are:

$$L_P = L_G = 0 \qquad [0.3]$$

$$R_G\text{ (ohms)} = R_T N \quad \text{from equation [0.2]} \qquad [0.4]$$

$$C_p\text{ (pF)} = \frac{\varepsilon_r \varepsilon_0 S}{H} = \frac{0.225 \times 10^{-6} \varepsilon_r S}{H} \qquad [0.5]$$

where:

R_T = Power plane resistance
N = Number of squares
S = Plane area
H = Plane separation
ε_0 = Permeability of Free Space

5.1.3.4 Device Output Load Models The signal line load will have two configurations: capacitive line and transmission line. A capacitive load requires a triangular current pulse at the rate of the output edge transition rate. The current pulse will only occur during the transition.

The transmission line load behaves resistively to the incident signal. The output provides a trapezoidal pulse to the line while the transmission line is active. The I_{cc} requirements have this trapezoidal waveform versus a triangular waveform for a capacitive load. The I_{cc} waveforms for capacitive and transmission line loads are shown in Figure 5-5. Figure 5-6 presents the Fourier Transform for the waveform presented in Figure 5-5.

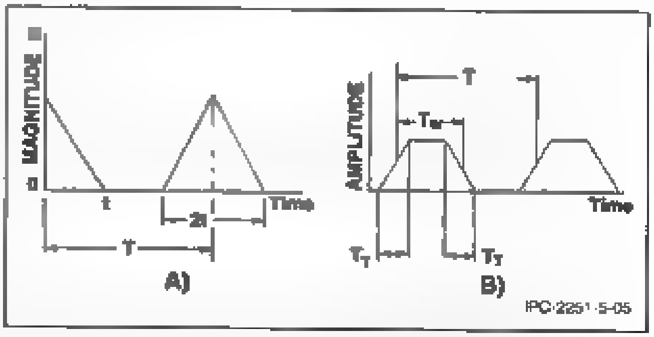


Figure 5-5 Capacitive and Transmission Line Current Pulses – A) is for a very short line and B) is for a long line

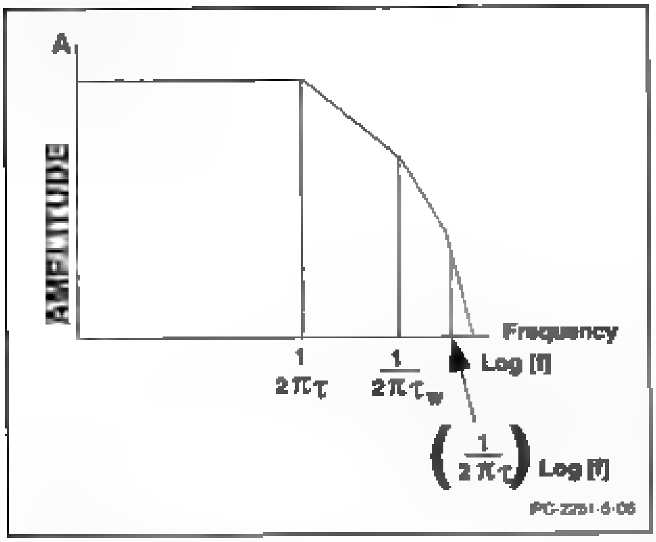


Figure 5-6 Fourier Transform

5.1.4 Decoupling Capacitance and Plane Capacitance

Decoupling capacitors and Plane Capacitance provide current to devices until the power supply can respond. High frequency switching, which is composed of a broad spectrum of very high frequencies, and requires plane capacitance to support them. The discrete capacitors recharge the plane capacitors.

5.1.4.1 Switching Transient Capacitance Switching transient capacitance provides very fast energy to charge the output sections of the device during an output transition This transient typically contains the highest frequency content of the power to the device but the least amount of energy. With modern devices, this current may be tens to hundreds of amps at the edge rate. Sometimes, this energy requirement is aided by chip capacitance in the form of discrete component capacitors or as part of the package power interconnect (BGA Carrier). Including the decoupling capacitance in the package minimizes the lead inductance between the capacitance and the device that requires the local energy. This capacitance is almost always not enough for the device and additional capacitance must be provided external to the device. If insufficient energy is available, the signal transition time will degrade prior to leaving the device package. The second effect is high frequency ripple currents appear on the Vdd/Vcc rails and planes, which can result in higher levels of EMI.

In high-speed applications, it is necessary to provide a PWB structure where a Power Plane and a Ground Plane are placed adjacent to each other in the stack-up to provide additional capacitance. This structure generally forms a plate capacitor sometimes referred to as buried capacitance. In this structure there is typically less than 0.127 mm [0.005 in] of dielectric thickness between the power and ground planes. The buried capacitance provided by the planes provide high speed switching current prior to the current being supplied by the discrete high frequency decoupling capacitors. This buried plane capacitance is increased as the planes are spaced closer together or the dielectric constant of the PWB board material is increased. There may be a limit to how close the planes may be placed as far as reliability is concerned. Actual copper plane material is not completely smooth. During the PWB manufacturing process, it is polished for manufacturability, which improves the surface finish. There still remain very small spurs that protrude into the dielectric material between the planes. With smaller dimensions between the planes, a small conductive filament develops that may cause a plane short. This is referred to as Electro migration, Conductive Filament Formation (CFF), or Conductive Anodic Filament (CAF). This starts as a chemical and environmental problem at first and when a voltage bias is applied, the filaments grow from each plane through the dielectric until they complete the shorting filament and cause a short between the planes. Some dielectric materials are less susceptible to the problem. This may also occur with Plated-Through Holes (PTH) as well.

5.1.4.2 Line Charging Capacitance or High Frequency Decoupling Line charging capacitance provides switching current to charge the signal line after the signal reaches the lines. The charge current is required until the line reaches its quiescent state. If insufficient current is provided to the device, the edge transition time will degrade or become noisy.

5.1.4.3 Low Frequency (Bulk) Capacitance Low frequency capacitance is often termed bulk capacitance. This capacitance is used to recharge power planes and higher frequency charging capacitors, and provide switching current for lower frequency requirements. Generally, bulk capacitance is placed at each voltage input to the board. It is also distributed on the board using an "area of influence" method to supply the high frequency decoupling local charge current.

5.1.4.4 Capacitor Model The model for a packaged capacitor is shown in Figure 5-7. R_L and L_L are the resistance and inductance of the capacitor leads, C_C is the ideal capacitance, R_C is loss of the capacitor, and R_{SH} is the resistance of the insulation. R_{SH} and R_C can be added in parallel to give R_P:

$$R_P = \frac{R_C R_{SH}}{R_C + R_{SH}} \qquad [0.6]$$

Using R_P, the impedance of the packaged capacitor is given by:

$$Z_C = R_L + j\omega L_L + \left(\frac{1}{R_P} + j\omega C_C\right)^{-1} \qquad [0.7]$$

$$R_L + j\omega L_L + \frac{R_P\,(1 + j\omega C_C R_P)}{1 + \omega^2 C_C{}^2 R_P{}^2} \qquad [0.8]$$

$$= R_L + \frac{R_P}{1 + \omega^2 C_C^2 R_L^2} + j\omega\left(L_L - \frac{C_C R_P^2}{1 + \omega^2 C_C^2 R_P^2}\right) \quad [0.9]$$

where $j\omega L_L$ and $\frac{1}{j\omega C_C}$ are the impedances of the inductance and capacitance associated with the packaged capacitor. At very low frequencies and for $L_L >> C_C R_P$, the packaged capacitor impedance, $Z_{C,lo\text{-}freq}$, can be approximated by:

$$Z_{C,lo\text{-}freq} \cong R_L + R_P + j\omega L_L \quad [0.10]$$

At high frequencies, the packaged capacitor impedance, $Z_{C,hi\text{-}freq}$, can be approximated by:

$$Z_{C,hi\text{-}freq} \cong R_L + j\omega\left(L_L - \frac{1}{\omega^2 C_C}\right) \quad [0.11]$$

Capacitors with shorter leads provide current faster because the lead inductance is much lower. In high-speed designs, changing the decoupling capacitors from leaded to leadless SMD capacitors can dramatically increase the circuit performance. The optimum scenario is when the capacitance can be provided within the component package, on the MCM, in the hybrid, or in the circuit board.

The lumped constant equivalent circuit of the capacitor is illustrated in Figure 5-7. R_{SH} is the insulation resistance and has a value >100 M ohms. It has minimal effect on the operation of the capacitor and will be omitted from further discussions. R_C (ESR) is the series resistance. L_C is composed of lead and plate inductance. C_C is the bulk capacitance of the capacitor. In a DIP capacitor the plate inductance is minimal relative to the lead inductance, which is approximately 10 nH/in.

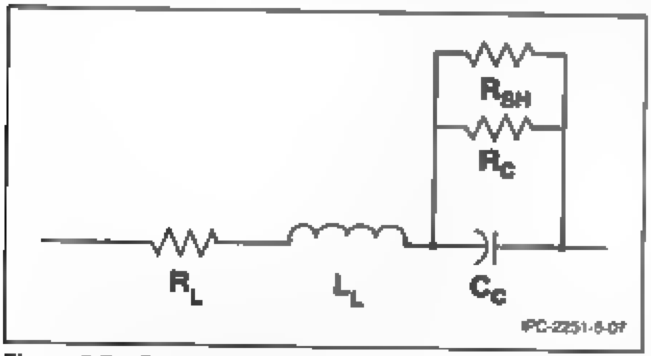


Figure 5-7 Capacitor Equivalent Circuit

The total effective impedance, ZC of the capacitor is:

$$Z_C \text{ (ohms)} = \sqrt{R_L^2 + (X_L - X_C)^2} \quad [0.12]$$

where:

R_L is the series lead and plate resistance

$$X_L = 2\pi f L_C \quad [0.13]$$

$$X_C = \frac{1}{2\pi f C_C} \quad [0.14]$$

The series inductance and capacitance yield a resonant frequency at which the effective impedance will equal the series lead resistance, R_C. Below resonance Z_c is dominated by the capacitive reactance. Above resonance Z_c is primarily inductive reactance. Impedance values for 0.1 µF and 0.01 µF DIP and 1206 style capacitors are presented in Table 5-3.

Table 5-3 Impedance for 0.1 µF and 0.001 µF DIP and 1206 Capacitors

F	DIP Style				1206 Style			
	0.1 µF		0.01 µF		0.1 µF		0.01 µF	
MHz	X_L	X_c	X_L	X_c	X_L	X_c	X_L	X_c
10	0.6	0.16	0.5	1.6	0.1	0.16	0.1	1.6
100	5.9	0.016	4.7	0.16	1.2	0.016	1.2	0.16
150	8.9	0.011	7.1	0.10	1.9	0.011	1.9	0.10
200	11.8	0.008	9.4	0.08	2.5	0.008	2.5	0.08
300	17.6	0.005	14.0	0.05	3.8	0.005	3.8	0.05
350	20.7	0.004	16.5	0.05	4.4	0.004	4.4	0.05
400	23.4	0.004	18.7	0.04	5.0	0.004	5.0	0.04
L_C (nH)	9.4		7.5		2.0		2.0	
R_L (ohms)	0.065		0.15		0.065		0.15	

5.1.4.5 PWB Decoupling Recommendations There are varying philosophies for properly decoupling a board. Some prefer rules-of-thumb, which have worked in application, some use quantities of different values to cover frequency ranges, some prefer little distributed bulk decoupling, some prefer to decouple in an area-of-influence method. The best design is to provide the right range of values to provide a low enough impedance to cover the applicable frequency range, with the least amount of components. In the past, since widespread decoupling information was not available, rules-of-thumb were often used. This was acceptable in most situations due to the current technology of the drivers. Current technology demands a more methodical approach based on point-of-use current delivery. This means supplying the correct amount of current (or low impedance) where it is needed for the frequency range required. This requires the designer to understand the circuit requirements and develop a decoupling method that satisfies those requirements. The most important parameters that need to be known are frequency range, transient current, and target impedance of the PDS. Once the requirements are known, a network of capacitance may be designed to meet the requirements.

5.1.4.6 Point-Of-Use Delivery Methodology The Point-Of-Use Delivery method requires a good understanding of the entire board. Each circuit block is isolated and investigated then combined with other blocks until the complete board requirements are known. The PDS is then designed to meet these requirements. The designer calculates the current requirements from the expected driver currents, PCB impedance, receiver capacitance, the current requirements, and frequency range of each voltage rail investigated based on clock frequency.

5.1.4.7 Rules-of-Thumb Decoupling Methodology In the event that the design parameters may not be able to be known, the following recommendations may be applied to the design as rules-of thumb. Please consult vendor documentation for other recommendations.

a) Provide a parallel low frequency bulk capacitor (tantalum is preferred) and a high frequency capacitor (ceramic SMT is preferred) at the power input connector for each power supply. Typical values are 22 µF to 47 µF tantalum capacitor paralleled with a 0.1 µF ceramic capacitor. This will provide clean, low inductance power for the PWB and reduce EMI that can escape through power cabling. More than one set of capacitors may be required. It is recommended that a 0.1 µF capacitor be provided for unused power supply connector pins.

b) Provide local high frequency decoupling capacitors at each device power and ground pins or pin pair if common power pins are adjacent. Clock drivers, programmable logic devices, microprocessors and microcontrollers, interface cable drivers, ECL/GTL signal line termination resistor packs, and other devices may require multiple high frequency decoupling capacitors. Generally, 0.01 µF to 0.1 µF ceramic SMT capacitors work best when placed directly underneath the device on the backside of the board. As an alternate, capacitors may be placed on the topside with short, wide, closely spaced traces connected to the IC pins via'd into the planes. Many device manufacturers publish application notes and addendums recommending high frequency decoupling placement.

c) Provide distributed bulk low frequency and mid frequency decoupling capacitors near large programmable devices. Usually two to four capacitors each 4.7 µF to 22 µF tantalum capacitors on two opposite corners works well. In addition, 4.7 to 10 µF capacitors should be distributed throughout the board in an "area of influence" or "predicted current flow area" method. These bulk capacitors reduce plane inductance and provide charge energy for the high frequency decoupling capacitors. Some vendors recommend that large bulk (~470 µF) be placed locally for each large programmable device or processor to satisfy instantaneous current requirements. Some linear and switching power supply vendors require large amounts of low ESR bulk capacitance at the supply output and input.

d) Use short, wide traces for power and ground interconnections. Generally a 0.51 mm [0.020 in] trace-width works well when connecting a decoupling capacitor to a via. Use the widest trace possible for SMT pads on chips, a smaller width may be used to enter the SMT pad, but the trace should be expanded afterwards as soon as feasible. Manufacturing and assembly restrictions may restrict allowable trace widths to maintain solder integrity.

e) When carrying heavy currents, use large area, surface pads when connecting to high current pins. This large pad may connect to internal planes with multiple solid filled (no thermal tie leg) vias. Connecting a via with large pad and no thermal ties on more than two planes causes solderability problems during solder reflow. Use care when selecting via inside plating thickness and via spacing to calculate current transfer from the pad to planes. Use the current nomographs in IPC-2221 as a guide for current calculations. This pad is sometimes referred to as a power pad or patch, and manufacturing may have restrictions on its use, via size, and number of vias.

f) Use solid filled vias or wide thermal ties on vias connecting capacitors, large wattage resistors, power isolation ferrite beads, and power jumper traces to maximize current transfer. Four thermal ties, 0.38 mm [0.015 in] wide, work well in most applications that require thermal ties.

Some applications require decoupling for isolation between noise sensitive circuitry. Examples of this are analog where isolated bulk and high frequency decoupling may be necessary. Transmitters and receivers such as fiber optic devices may require isolated decoupling. For these situations, it is recommended that each be treated with individual requirements. Receiver power is typically isolated from transmitter power to prevent cross-modulation. In some devices, the input receiver requires power isolation from the on chip output buffers. Isolate the receivers with a high value, low DC series resistance inductor. Decouple the receiver with both high frequency and low frequency bulk decoupling. Provide separate high frequency and low frequency bulk decoupling for the receiver output buffer. RF devices, PLLs, VCOs, and frequency sensitive devices need additional attention to decoupling. These situations usually require creating a separate isolated supply with individual linear regulators or a specially filtered supply. The regulators provide high isolation (up to 60 dB) and additional high frequency and low frequency bulk decoupling will be necessary. The low frequency bulk decoupling is especially effective to reduce jitter and phase noise in PLL and VCO applications. Care must be taken to avoid resonance with inductance and capacitance values. Many device manufacturers provide application notes for special decoupling requirements.

5.1.5 Device Power Dissipation The system power dissipation can be calculated by the addition of the component power dissipations. For example, the power dissipation categories are:

1. Bipolar SSI/MSI
2. CMOS SSI/MSI

5.1.5.1 Bipolar SSI/MSI The power dissipation in bipolar SSI/MSI devices has three primary components:

1. I_{ccl} and I_{cch} steady state
2. Output load charging current, I_{cl}
3. Internal dynamic charging

5.1.5.1.1 I_{ccl} and I_{cch} Steady State Currents The values for I_{ccl} and I_{cch} are obtained from the vendor data sheets. The nominal value of I_{cc} is calculated to be the average of I_{ccl} and I_{cch}. For a statistically accurate worst-case analysis, 10% above typical values, at a 50% duty cycle, are used. The value for the worst-case power dissipation may be calculated from the following equations, where the values of I_{ccl} and I_{cch} vary by 10%.

$$I_{cc,dc} = \frac{1.1}{2}(I_{ccl,\,nom} + I_{cch,\,nom}) \qquad [0.15]$$

$$= 0.55\,(I_{ccl,\,nom} + I_{cch,\,nom}) \qquad [0.16]$$

or,

$$P_{cc,dc}\,(mW) = V_{cc,\,nom}\,I_{cc,\,nom} \qquad [0.17]$$

5.1.5.1.2 ICL To compute the OSLCC (I_{cl}), for a worst-case analysis, use the maximum possible outputs switching at a given time driving their statistically maximum loads. The following decoupling analysis shows that the capacitive load charging current can be approximated as triangular in shape. Thus,

$$I_{CL}\,(A) \quad 0.5C_L\left(\frac{dV_C}{dT}\right) \qquad [0.18]$$

$$I_{CL}\,(A) \quad 0.5\,C_L\left(\frac{V_{OH} - V_{OL}}{T_{LH}}\right) \qquad [0.19]$$

and,

$$P_{CL} = (V_{out.\,nom} - V_{OH})\,I_{CL}N \qquad [0.20]$$

$$P_{CL} = (V_{CC,\,nom} - V_{OH})\,I_{CL}N \qquad [0.21]$$

where:

I_{CL} = Load charging current
C_L = Load capacitance
$\frac{dV_C}{dT}$ = Output edge transition rate
V_{OH} = Voltage out high
V_{OL} = Voltage out low
T_{LH} = Edge transition time
P_{CL} = Device power dissipation due to load
N = Number of device loads

5.1.5.1.3 Internal Dynamic Charging As the system clock frequency increases the dynamic power dissipation will increase due to the inherent device capacitance. Vendor data provides the power increase with frequency.

5.1.5.1.4 Total Power Requirements Total power requirement is:

$$P_{TOT} = K_D\,(P_{cc,dc} + P_{CC}) \qquad [0.22]$$

where:

K_D = Switching frequency multiplier

5.1.5.2 CMOS Power consumption for CMOS is dependent on the power supply voltage, frequency of operation, internal capacitance, and load. The power consumption may be calculated for each package by summing the quiescent power consumption, $I_{CC}V_{CC}$, and the switching power required by each device within the package. The device dynamic power requirements can be calculated by the equation:

$$P_D = (C_L + C_{PD})\,(V_{CC})^2\,f \qquad [0.23]$$

See vendor data for calculating power dissipation in CMOS devices.

5.2 Permittivity

5.2.1 Relative Permittivity The relative permittivity, ε_r, of a substance is defined as the ratio of the permittivity of the material to that of free space. The term relative Permittivity is preferred to dielectric constant, since this quantity is not a constant, but varies with several parameters. Factors that influence the relative Permittivity of a given material include: the electrical frequency at which the measurement is performed, temperature and extent of water absorption. In addition, if the material is a composite e.g., a reinforced laminate, the value of ε_r may vary enormously as the relative amount of each component of the composite is changed.

5.2.2 Effective Relative Permittivity The effective relative permittivity, $\varepsilon_{r,eff}$, is the relative permittivity that is experienced by an electrical signal transmitted along a conductive path. An experimental value of $\varepsilon_{r,eff}$ may be obtained using a time domain reflectometer (TDR) technique. However, it is frequently more convenient to calculate a value of $\varepsilon_{r,eff}$ from known values of ε_r.

If a stripline signal conductor is surrounded by a single dielectric that extends to the ground planes, then the value of $\varepsilon_{r,eff}$ may be equated to that of ε_r for the dielectric measured under the appropriate conditions. However, if more than one dielectric is present between the conductor and the ground planes, a value of $\varepsilon_{r,eff}$ is determined from a weighted sum of values of ε_r for all the contributing dielectrics. For the purposes of evaluating electrical characteristics of circuit boards, a composite such as a reinforced laminate, with a given ratio of components, is usually regarded as a homogeneous dielectric with an associated relative permittivity.

Some typical electrical configurations are illustrated in Figure 5-8. If a single dielectric is employed, then the value of $\varepsilon_{r,eff}$ is taken to be the value of ε_r for that dielectric, but for the remaining structures the situation is more complex.

The microstrip case, Figure 5-8 (c), has a compound dielectric medium consisting of the board material and air. For this configuration, an empirical relationship has been derived (Kaupp, 1967) that gives the effective relative permittivity as a function of the relative permittivity of the board material.

$$\varepsilon_{r,eff} = 0.475\,\varepsilon_r + 0.67 \text{ for } 2 < \varepsilon_r < 6 \qquad [0.24]$$

In this expression ε_r relates to values determined at 25 MHz; see the next section for details of frequency dependence.

For electrical configuration (d), the coated microstrip, the following relationship (of unknown origin) is believed to be applicable:

$$\varepsilon_{r,eff} = \varepsilon_r\left(1 - e^{\left(-1.55\frac{h'}{h}\right)}\right) \qquad [0.25]$$

where:

h = The distance from the reference plane to the signal line

h' > h + t

h'= The distance from the reference plane to the top of the dielectric.

For the wire-over-ground (b) configuration, if the dielectric medium extends from the ground plane beyond the conductor, then the latter expression may be employed. If, however, the dielectric extends only to the level of the conductor, then either the latter expression or the relationship derived by Kaupp may be applied.

Unfortunately, none of the relationships provided in this section are applicable to circuit boards constructed of two or more dielectric materials (excluding air), such as microstrip circuitry coated with solder mask, or printed boards fabricated with more than one type of laminate, or discrete wiring boards with their polyimide insulated wires.

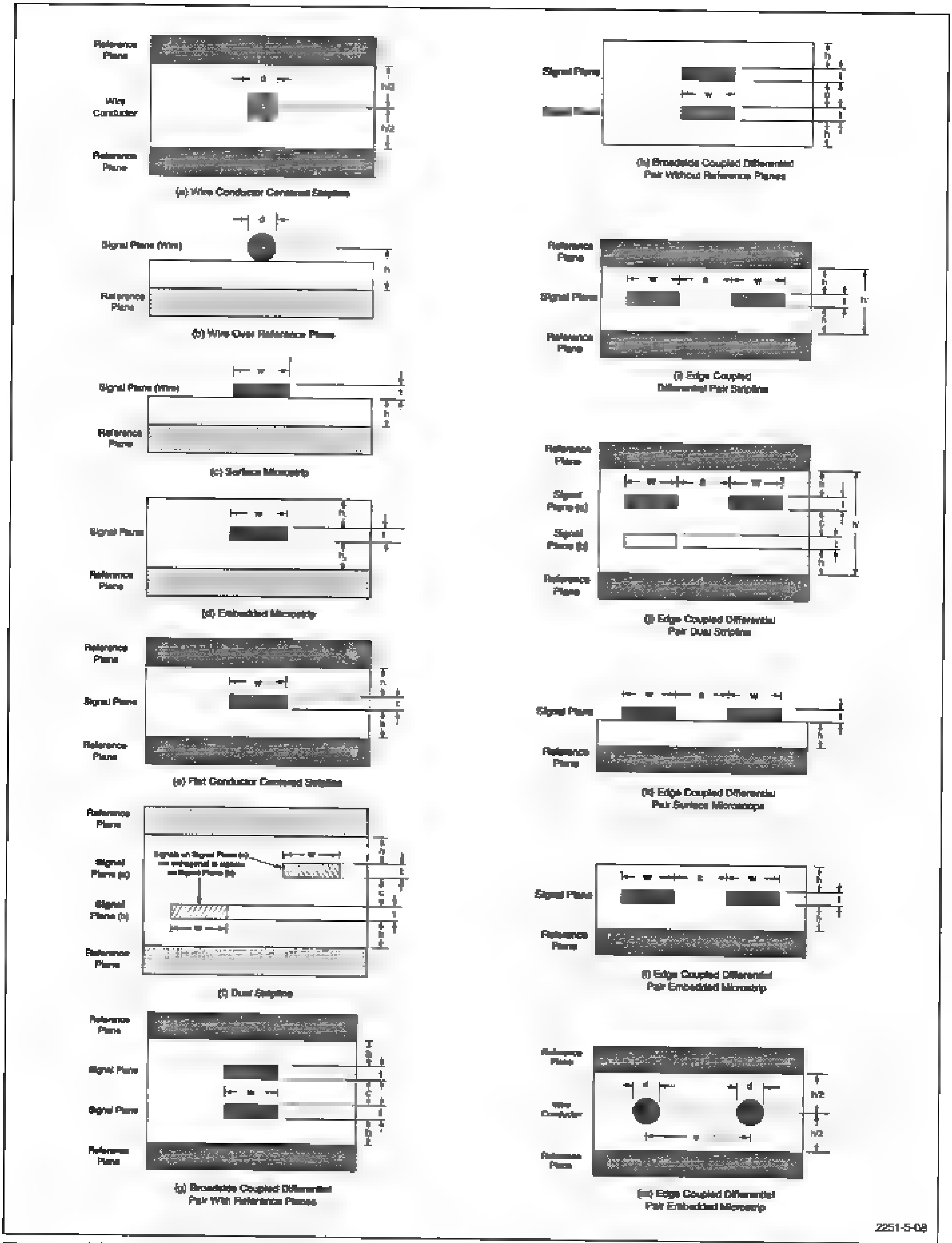
5.2.3 Frequency Dependence As has been explained in the preceding section, values of both ε_r and $\varepsilon_{r,eff}$ are dependent not only on the material employed, but also on the reinforcement-to-resin ratio (if a composite), temperature, water uptake and the frequency at which the measurement is performed. Once these dependencies are appreciated, steps may be taken to ensure that electrical measurements are performed under conditions that are pertinent to the final application. However, the frequency dependence of ε_r and $\varepsilon_{r,eff}$ is worthy of further comment, since it is not usually obvious at what frequency measurements should be performed.

Some materials, such as an FR-4 epoxy/glass laminate, exhibit a significant frequency dependence of their dielectric properties, and it becomes important to choose carefully the frequency at which measurements are made. It is essential not only to maintain internal consistency, but also to select the frequency such that the dielectric parameters obtained may be used to provide a precise prediction of the electrical characteristics of the finished circuit board. Since most transmission characteristics for a circuit board are determined by TDR measurements, it is appropriate to use the frequency corresponding to these TDR measurements as the frequency of choice for comparing dielectric parameters. Although TDR is a wideband technique and measurements are performed in the time domain, an approximate frequency may be associated with values determined in this manner. Values of $\varepsilon_{r,eff}$, for instance, are determined from the propagation time, but locating the precise position on the TDR output that corresponds to the end of the conductor is frequently subjective. However, if the end point of the conductor is determined in the usual way, from the divergence of two TDR curves recorded with the signal line terminated by an open and a short, then the resulting value of $\varepsilon_{r,eff}$ corresponds to the highest frequency component of the TDR pulse. The highest frequency of concern, or bandwidth (BW) in Gigahertz, of a digital pulse may be approximated by:

$$BW_{(GHz)} = \frac{0.35}{t_r\,(ns)} \qquad [0.26]$$

where, t_r in nanoseconds is the pulse rise time from 10% to 90% of its maximum value. Thus, a typical TDR pulse, with a rise time of 100 ps (25 ps at the probe tips), has a bandwidth of 3.5 GHz. (Some degradation of this risetime, however, occurs in transmission through the test fixture, thus reducing the effective frequency.) This dictates that dielectric measurements made by methods other than TDR must be conducted at high frequency.

Figure 5-9 shows plots of the relative Permittivity and loss tangent, measured over the frequency range 1 kHz to 1 GHz, for an FR-4 type laminate with a glass-to-resin ratio of approximately 40:60 by weight. The value of ε_r for this laminate varies from about 4.7 to 4.0 over this frequency


Reference Plane
Wire Conductor
Signal Plane (Wire)
Signal Plane
Signal Plane (a)
Signal Plane (b)
Signals on Signal Plane (a) are orthogonal to signals on Signal Plane (b)
d
w
s
h
h/2
h'
t
c
2251-5-08

(a) Wire Conductor Centered Stripline

(b) Wire Over Reference Plane

(c) Surface Microstrip

(d) Embedded Microstrip

(e) Flat Conductor Centered Stripline

(f) Dual Stripline

(g) Broadside Coupled Differential Pair With Reference Planes

(h) Broadside Coupled Differential Pair Without Reference Planes

(i) Edge Coupled Differential Pair Stripline

(j) Edge Coupled Differential Pair Dual Stripline

(k) Edge Coupled Differential Pair Surface Microstrips

(l) Edge Coupled Differential Pair Embedded Microstrip

(m) Edge Coupled Differential Pair Embedded Microstrip

Figure 5-8 (a) through (m) Typical Impedance Structures

range. This change in the magnitude of ε_r is principally due to the frequency response of the resin and thus is reduced if the proportion of glass in the composite is increased. In addition, the frequency response of ε_r will also be changed if an alternative resin system is selected. Material suppliers typically quote values of dielectric properties determined at 1 MHz. However, referring to Figure 5-9, the value of ε_r (4.4) at 1 MHz is some 10% higher than the more appropriate value (4.0) at 1 GHz. Consequently, use of the 1 MHz value of ε_r to calculate the propagation time or the characteristic impedance would result in a systematic error of approximately 5%. However, if a dielectric were selected that has a much reduced frequency response, such as PTFE, the question of frequency dependence of dielectric parameters becomes insignificant.

An exception to using high frequency values of ε_r, to estimate values of $\varepsilon_{r,eff}$ and subsequently calculate transmission characteristics, occurs when using empirical formulae based on measurements at a particular frequency. This is the case for the relationship given by Kaupp, which is based on measurements made at 25 MHz (typical edge rates are 250 MHz to 3500 MHz). Under such circumstances, values of ε_r should be used that have been determined at a frequency as close as possible to that used in establishing the original expression.

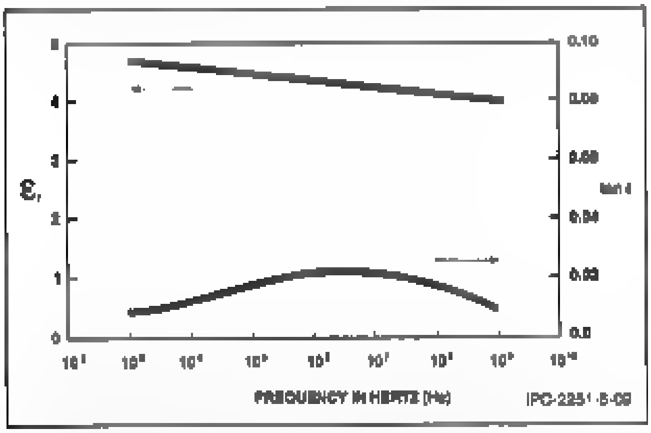


Figure 5-9 ε_r **and tan δ versus frequency for FR-4**

5.3 Lumped Capacitance Versus Transmission Line Environment At low frequencies, a signal path on a circuit board may usually be represented electrically as a capacitance in parallel with a resistance. However, as the frequency is increased, this approach of lumped circuit modeling breaks down and signal paths must be regarded as transmission lines. For transmission line interconnects, the electrical and dielectric properties of the board materials have an enhanced importance and greater care must be taken with the design and termination of the circuit. Several attempts have been made to define the point at which conductors act as transmission lines, the required analysis being performed in either the frequency or the time domain. However, the critical point to remember for digital signals is that it is the pulse rise or fall time, and not the rate at which the device is clocked, that is a key determining factor. Of course, the clock rate is a dependent parameter since the faster the rise time the faster a device can be clocked.

In the frequency domain, to obtain the point at which a conductor carrying a digital pulse must be regarded as a transmission line, first consider the Fourier components of the pulse and obtain the highest frequency of concern, or bandwidth (BW), from equation [0.26].

This bandwidth may then be used to calculate a corresponding wavelength in free space, and a consequently reduced wavelength in the dielectric of interest. A comparison is then made between this later wavelength and the length of the circuit conductor. For digital circuitry, if the circuit conductor length is greater than one seventh of the wavelength then the conductor typically must be considered a transmission line (Figure 5-8). (For analog circuitry, which is less tolerant of noise, the critical conductor length is usually shortened to one fifteenth of the wavelength in the dielectric medium.) Table 5-4 lists Logic family typical device rise and fall times, the corresponding bandwidth, critical length for microstrip and stripline, output currents, input thresholds, and propagation delay in FR-4 at the fastest edge rate. The data in the table provides an easy snapshot of logic families for designers. Most Programmable Logic has this data listed in data manuals and, since the technology changes so rapidly, the data manuals should be used for this data.

However, an alternative equivalent definition of the point at which a circuit board significantly affects the transmission characteristics of a propagating pulse, one that is conceptually more straightforward for digital systems and more widely cited within the circuit board community, compares the rise time to the path length without transforming into the frequency domain. The premise is to determine, for the transmission of a pulse of a given rise time, how long a conductor may be before a significant voltage difference is realized along its length. Conductors longer than this critical value are then regarded as transmission lines. Initially, the rise distance, S_r, in the dielectric of concern is calculated from the device rise time and effective relative Permittivity of the medium.

For a microstrip:

$$t_{pd}\,(\text{ps/inch}) = 1000\left(\frac{1.017\sqrt{0.457\varepsilon_r + 0.67}}{12\,(\text{inch})}\right) \qquad [0.27]$$

$$t_{pd}\,(\text{ps/mm}) = 1000\left(\frac{1.017\sqrt{0.457\varepsilon_r + 0.67}}{304.8\,(\text{mm})}\right) \qquad [0.28]$$

For a stripline:

$$t_{pd}\,(\text{ps/inch}) = 1000\left(\frac{1.017\sqrt{\varepsilon_r}}{12\,(\text{inch})}\right) \qquad [0.29]$$

Table 5-4 Typical Data for Some Logic Families

Logic Family	Typical Edge (nS)		Band Width Frequency	Critical Length				Output Drive Current (mA)		Logic Input Threshold		Typical Buffer Prop. Delay
				Microstrip		Stripline						
	Rise	Fall	(MHz)	in	cm	in	cm	I_{OL}	I_{OH}	V_{IL}	V_{IH}	
AGP	0.350	0.450	1000	0.63	1.60	0.50	1.27	20	-12	1.12	1.52	1.5 nS
BICMOS 74ABT	1.6	1.4	250	2.5	6.3	2.0	4.9	64	-32	1.1	1.9	3.6 nS
BICMOS 74BCT	0.700	0.700	500	1.24	3.15	0.98	2.49	64	-15	0.8	2.0	2.5 nS
BICMOS 74LVT	2.7	2.8	130	4.80	12.2	3.8	9.8	64	-32	1.3	1.7	4.1 nS
CMOS 74AC	1.7	1.5	233	2.7	6.8	2.1	5.3	24	-24	2.2	3.0	7.5 nS
CMOS 74ACT	1.7	1.5	233	2.7	6.8	2.1	5.3	24	24	0.4	2.1	10.0 nS
CMOS 74ACQ	2.4	2.4	146	4.3	10.8	3.4	8.4	24	-24	2.3	2.9	9.5 nS
CMOS 74ACTQ	2.5	2.4	146	4.3	10.8	3.4	8.4	24	24	1.2	2.0	7.0 nS
CMOS 74AHCT	2.4	2.4	146	4.3	10.8	3.4	8.4	24	15	0.8	2.0	7.0 nS
CMOS 74C	35.0	25.0	14	44.4	112.5	35	87.5	12	14	0.7	3.5	70.0 nS
CMOS 74FCT	1.5	1.2	292	2.1	5.4	1.7	4.2	64	15	0.8	2.0	3.1 nS
CMOS 74HC	3.6	4.1	97	6.4	16.2	5.0	12.6	6	-6	2.3	2.4	25.0 nS
CMOS 74HCT	4.6	3.9	90	6.9	17.6	5.5	13.7	6	-6	1.3	1.4	25.0 nS
CMOS 74LCX	2.9	2.4	146	4.3	10.8	3.4	8.4	24	24	1.3	1.8	6.5 nS
CMOS 74LV	3.0	3.0	116	5.3	13.5	4.2	10.5	8	-8	0.9	2.3	7.5 nS
CMOS 74LVQ	3.5	3.2	109	5.7	14.4	4.5	11.2	12	12	1.6	1.7	9.5 nS
CMOS 74LVX	4.8	3.7	95	6.6	16.7	5.2	13.0	4	-4	1.4	1.7	12.0 nS
CMOS 74VHC	4.1	3.2	109	5.7	14.4	4.5	11.2	8	-8	2.1	2.8	8.5 nS
CMOS 74VCX	2.0	2.0	175	3.6	9.0	2.8	7.0	24	-24	0.8	2.2	2.5 nS
CTT	0.600	0.750	583	1.07	2.70	0.84	2.10	8	-8	1.3	1.7	2.0 nS
ECL 10K	2.2	2.2	159	3.9	9.9	3.1	7.7	50	-50	-1.7	-0.95	2.0 nS
ECL 10KH	1.7	1.7	206	3.0	7.7	2.4	6.0	50	-50	-1.7	-0.95	1.0 nS
ECL 100K	0.600	0.600	583	1.07	2.70	0.84	2.10	50	-50	-1.5	-0.90	0.800 nS
ECL 300K	0.500	0.500	700	0.89	2.25	0.7	1.25	50	-50	-1.7	-0.95	1.55 nS
ECL (E)	0.375	0.375	933	0.67	1.69	0.53	1.31	50	-50	3.3	4.0	0.300 nS
LVPECL (EP)	0.110	0.110	3182	0.20	0.50	0.15	0.39	50	-50	1.6	2.4	0.160 nS
LVPECL (LVEL)	0.220	0.220	1591	0.39	0.99	0.31	0.77	50	-50	1.6	2.4	0.300 nS
PECL (EL)	0.225	0.225	1556	0.40	1.01	0.32	0.79	50	-50	3.3	4.0	0.250 ns
RSECL (SiGe-3.3V)	0.030	0.030	11700	0.06	0.14	0.04	0.11	25	-25	1.9	2.3	0.120 nS
RSECL (SiGe-2.5V)	0.030	0.030	11700	0.06	0.14	0.04	0.11	25	-25	1.1	1.5	0.120 nS
GaAs	0.300	0.100	3500	0.18	0.45	0.14	0.35	30	-30	0.8	2.0	0.250 nS
GTL	1.2	1.2	292	2.1	5.4	1.7	4.2	40	-40	0.75	0.85	3.0 nS
GTL+	0.300	0.300	1167	0.53	1.35	0.42	1.05	40	-40	0.80	1.20	3.0 nS
HSTL	0.620	0.220	1591	0.39	0.99	0.31	0.77	8–48	-8–48	0.75	0.85	1.7 nS
LVDS	0.300	0.300	1167	0.53	1.35	0.42	1.05	3.5	-3.5	1.07	1.41	2.0 nS
SSTL	0.330	0.510	1060	0.59	1.50	0.46	1.17	8–20	-8–20	1.30	1.70	1.8 nS
TTL 74	8.0	5.0	70	8.9	22.5	7	17.5	16	-15	0.8	2.0	20.0 nS
TTL 74ALS	2.3	2.3	152	4.1	10.4	3.2	8.1	24	-15	0.8	1.6	10.0 nS
TTL 74AS	2.1	1.5	233	2.7	6.8	2.1	5.3	64	-15	0.5	1.9	6.2 nS
TTL 74F	2.3	1.7	206	3.0	7.7	2.4	6.0	64	-15	0.9	1.8	6.5 nS
TTL 74FR	2.1	1.5	233	2.7	6.8	2.1	5.3	64	-15	0.6	2.2	3.9 nS
TTL 74H	7.0	7.0	50	12.4	31.5	9.8	24.5	20	-0.25	0.8	2.0	15.0 nS
TTL 74L	35.0	30.0	12	53.3	135.0	42.0	105.0	2	-0.4	0.8	2.0	35.0 nS
TTL 74LS	15.0	10.0	35	17.8	45.0	14.0	35.0	24	-15	0.8	1.8	18.0 nS
TTL 74S	2.5	2.0	175	3.6	9.0	2.8	7.0	64	-15	0.8	1.8	6.0 nS

$$t_{pd}\text{ (ps/mm)} = 1000\left(\frac{1.017\sqrt{\varepsilon_r}}{304.8\text{ (mm)}}\right) \qquad [0.30]$$

$$S_r\text{ (meters)} = \frac{t_r}{\sqrt{\varepsilon_{r,eff}}} \qquad [0.31]$$

This is for 10 to 90% of the rise

where:

S_r = Trace Length (m)
t_r = Signal rise time (s)
$\varepsilon_{r,eff}$ = Relative Permittivity (Dielectric Constant) at fastest edge speed

If circuit lengths are equal or greater than $0.5S_r$, then the circuit is regarded as a transmission line, i.e., if the maximum voltage drop is greater than half the pulse height value. The choice of $0.5S_r$ to determine the maximum path length before the onset of transmission line characteristics is somewhat arbitrary. Some engineers choose to specify $0.2S_r$ to $0.5S_r$ as the maximum path length depending on whether the line has distributed loading or not. The selection is based on how conservative the design rules are. The Critical Electrical Lengths in Table 5-4 were calculated using $0.25S_r$ with an FR-4 Dielectric Constant for the fastest edge rate. The Dielectric Constant used for the calculations was 4.0 (refer to Figure 5-9). The trace propagation delay used for the Microstrip calculations was 140 ps/in (refer to Equation [0.49]). The trace propagation delay used for the stripline calculations was 180 ps/in (refer to equation [0.54]). The trace length is important due to other practical considerations: For path lengths longer than $0.5S_r$, reflections from a mismatched load impedance may be received back at the source after the pulse has reached its maximum plateau value, and pulse additions that occur under these circumstances may lead to false triggering of a device caused by a nonmonotonic edge. For path lengths shorter than $0.5S_r$, however, reflected pulses are received back at the source before the pulse has reached its plateau value. Therefore, any modification of the pulse shape will only be to the leading edge, which is less likely to produce false device triggering. It has been suggested that circuit conductors longer than $0.3S_r$ be regarded as transmission lines and these more stringent criteria allow a greater margin for error. However, irrespective of the precise definition that is used, the point at which a circuit becomes a transmission line is not defined by a single variable, but by the interplay of device rise time, conductor path length, load topology, and the relative Permittivity of the medium. Once we enter the realm of effective transmission line design, close attention must be paid to the models described in the following sections. Many devices have programmable drive strengths and slew rates, careful attention must be paid to the rise and fall time of the programmed device output characteristics. Many devices support multiple logic family interface standards i.e., TTL, LVTTL, CMOS, LVCMOS, GTL, GTL+, HSTL, SSTL, CTT, AGP, etc., logic families. Those devices may have separate supply voltages and comparator references for groups of I/O pins that will need to be considered. IBIS and SPICE models provide some of this information and design tools may require application programmed device specific models for proper circuit simulation.

5.4 Propagation Delay Time

5.4.1 Capacitive Line When the signal line is considered a capacitive line the propagation time is calculated assuming the line plus the loads connected to it are purely capacitive (see Figure 5-10).

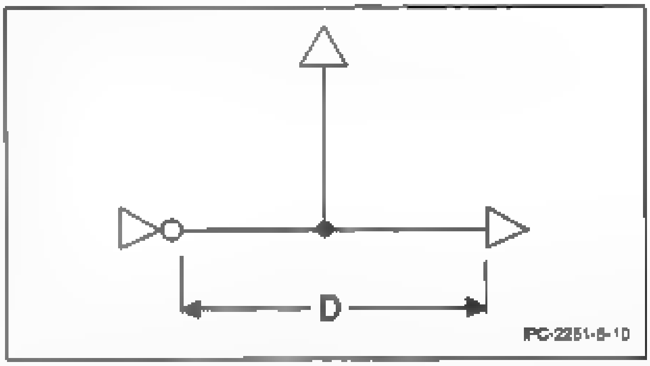


Figure 5-10 Capacitive Loading

Because the reflections on the short interconnecting line occur several times during the pulse's rise time, the net result is a degradation of the edge transition time, i.e., slowing down, versus distinct steps that occur in transmission lines.

Using the transmission line equations generally provides a much faster propagation time, creating an inaccurate result.

5.4.2 Transmission Line Using Maxwell's equations, it may be shown that the speed of light in a vacuum, c, is related to the absolute permittivity and absolute permeability of a vacuum, ε_o and μ_o, respectively, by:

$$c = \frac{1}{\sqrt{\varepsilon_o \mu_o}} \qquad [0.32]$$

More generally, for the velocity of propagation, V_p, of a wave in a homogeneous dielectric:

$$V_p = \frac{1}{\sqrt{\varepsilon\mu}} \qquad [0.33]$$

where:

ε = The absolute permittivity of the dielectric and
μ = The absolute permeability of the dielectric.

Since the dielectrics employed in the fabrication of circuit boards are not ferromagnetic in nature, μ may usually be taken to be equivalent to μ_o. Consequently, the propagation delay time, t_{pd}, of a signal traveling through a conductor surrounded by a homogeneous, nonferromagnetic medium, is given by:

$$t_{pd} = \sqrt{\varepsilon \mu_0} \quad [0.34]$$

$$t_{pd} = \frac{\sqrt{\varepsilon}}{c\sqrt{\varepsilon_0}} \quad [0.35]$$

therefore,

$$t_{pd} = \frac{\sqrt{\varepsilon_r}}{c} \quad [0.36]$$

For a signal passing through a conductor in a circuit board, where more than one dielectric may be present, it is more appropriate to substitute $\varepsilon_{r,eff}$ for ε.

$$t_{pd} = \frac{\sqrt{\varepsilon_{r,eff}}}{c} \quad [0.37]$$

It may be seen that propagation delay time is directly proportional to the square root of the effective relative permittivity. In order to calculate the propagation time for a signal transmitted down a specific conductor, one must use equation [0.37] and refer to 5.2.2 if a value needs to be derived for $\varepsilon_{r,eff}$ from known values of ε_r for the surrounding dielectrics. Alternatively, one may consult 5.5.1, which lists a compilation of equations for several circuit configurations.

5.5 Impedance Models The characteristic impedance (Z_0) of a circuit line is analogous to the resistance of a DC circuit (given by Ohm's Law as R = V/I). For a high-speed circuit, the impedance is still the ratio of the driving voltage to the current that flows along the conductor. The critical difference is that in the high-speed case we are interested in the current flow during the very short period of time before the rising or falling edge of the voltage pulse reaches the next board component.

Circuit impedance is important in board design for several reasons. First, applying the definition above, it is apparent that the amount of current that a circuit element (driver) will need to pass along a signal path depends upon Z_0. This is taken into account in the design of ICs, and can affect how receivers may be placed along the circuit. (See 5.6 on circuit loading effects.) Second, in high-speed systems, any discontinuity along the path that a signal must travel will cause reflections. Reflections not only reduce the amount of power reaching the receiver, but also may cause ringing along the circuit. These forms of signal degradation can cause systems to malfunction due to missed signals (from attenuation) or due to spurious signals (from reflections).

Because the time period for measurement is very short (unlike the DC case), circuit termination does not affect the characteristic impedance (although it is very important in determining reflection characteristics). Likewise, the resistivity of the conductor material (typically copper) does not contribute significantly to the high-speed circuit impedance. Both of these effects are because the ratio of driving voltage to current flow (V/I = impedance) is determined before the signal reaches the end of the circuit.

The general equation for the characteristic impedance of a circuit is:

$$Z_0 = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}} \quad [0.38]$$

where:

Z_0 = characteristic impedance of circuit in ohms
R_0 = resistance per unit length of line [ohms]
L_0 = inductance per unit length of line [henrys]
G_0 = conductance per unit length of line [mhos]
C_0 = capacitance per unit length of line [farads]
$j = \sqrt{(-1)}$
$\omega = 2\pi f$, where (f = frequency in Hz)

At high frequencies, it is generally quite accurate to assume that ωL >> R and ωC >> G, so the equation [0.38] can be simplified to:

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \quad [0.39]$$

The following sections will present equations giving specific forms of the above general relation, for each special case. Refer to Appendix C for typical board constructions.

5.5.1 Microstrip An ideal microstrip transmission line consists of a narrow conductor separated from an infinite ground plane by a layer of dielectric material. In the simplest case (an uncoated line), the conductor sits on top of the dielectric, surrounded on the sides and top only by air. We will consider both round and rectangular conductors.

5.5.1.1 Wire Microstrip The characteristic impedance, in ohms, Z_0, of a single round wire near ground is given approximately by:

$$Z_0\,(\text{ohms}) = \frac{60}{\sqrt{\varepsilon_{r,eff}}} \ln\left(\frac{4h}{d}\right) \quad [0.40]$$

where h and d are as defined in Figure 5-11. A ground is the conductive plane on an adjacent layer

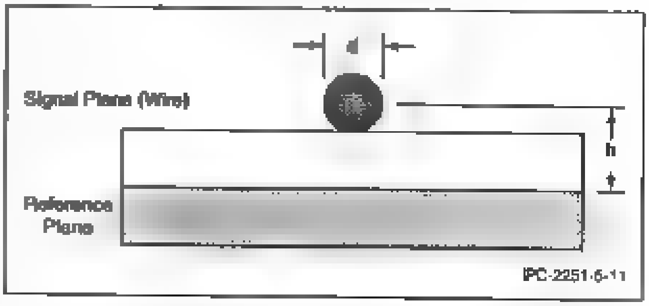


Figure 5-11 Wire Over Reference Plane

When no dielectric material is present, $\varepsilon_{r,eff} = \varepsilon_{r\,(air)} = 1$ However, for a circuit board, the conductor (wire) is supported from below by a dielectric material, and surrounded above by air. Consequently, $\varepsilon_{r,eff}$ is less than ε_r of the insulating support because the wire is only partially submerged in the support (see 5.2). An empirical relationship is:

$$\varepsilon_{r,eff} = \sqrt{0.475\,\varepsilon_r + 0.67} \text{ from equation [0.24]}$$

$$Z_0\,(\text{ohms}) = \frac{87}{\sqrt{(\varepsilon_r + 1.41)}} \ln\left(\frac{4h}{d}\right) \qquad [0.41]$$

where ε_r is the permittivity of the material between the wire and ground.

5.5.1.2 Flat Conductor Microstrip This is the geometry normally found on a printed circuit board as manufactured by copper plating and etching processes. Both the inductance and capacitance (per unit length) are modified from the round conductor case. The capacitance is influenced most strongly by the region between the signal line and adjacent ground (or power) planes. The inductance depends primarily upon an effective diameter that relates to the perimeter of the circuit.

An article was published in 1967 gives an excellent introduction to microstrip transmission lines [Kaupp, 1967]. The author starts with the equation for a wire over ground in air (as given in the previous section). By incorporating theoretical work and experimental measurements he derives the equations describing a rectangular circuit separated from a copper plane by a dielectric layer (see Figure 5-12).

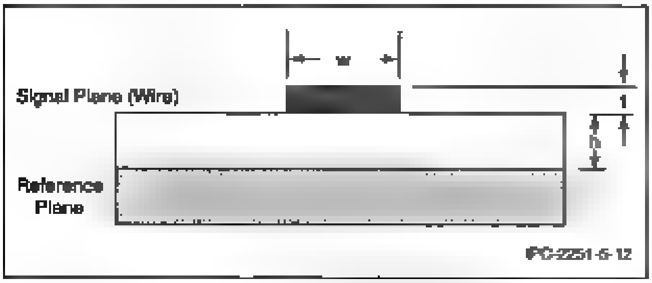


Figure 5-12 Flat Conductor Surface Microstrip

The following equations give the impedance (Z_0), intrinsic line capacitance (C_0), intrinsic line inductance (L_0), and intrinsic propagation delay (t_{PD}) for microstrip circuitry.

$$Z_0\,(\text{ohms}) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \qquad [0.42]$$

$$t_{pd}\,(\text{ps/inch}) = 1000\left(\frac{1.017\sqrt{0.457\,\varepsilon_r + 0.67}}{12\,(\text{inch})}\right) \qquad [0.43]$$

$$t_{pd}\,(\text{ps/inch}) = 84.75\sqrt{0.475\,\varepsilon_r + 0.67} \qquad [0.44]$$

$$C_0\,(\text{pF/inch}) = \frac{t_{pd}\,(\text{ps/in})}{Z_0\,(\text{ohms})} \qquad [0.45]$$

$$L_0\,(\text{nH/in}) = \frac{Z_0^2 C_0}{12} \qquad [0.46]$$

where:

h = Dielectric thickness
w = Line width
t = Line thickness

restrictions:

$$0.1 < \frac{w}{h} < 3.0$$

$$1 < \varepsilon_r < 15$$

The radiated electromagnetic signal (EMI) from the lines will be a function of the line impedance, the length of the signal line and the incident waveform characteristics. This may be an important consideration in some high-speed circuitry. In addition, cross talk between adjacent circuits (see 5.7) will depend directly upon circuit spacing and the distance to the power or ground plane.

5.5.2 Embedded Microstrip Coated microstrip has the same conductor geometry as the uncoated microstrip discussed above. However, the effective relative permittivity is different because the conductor is fully enclosed by the dielectric material. The equations for embedded microstrip lines are the same as in the section on [uncoated] microstrip, with a modified $\varepsilon_{r,eff}$. If the dielectric thickness above the conductor is several mils or more, then $\varepsilon_{r,eff}$ can be determined as in 5.2. For very thin dielectric coatings, the $\varepsilon_{r,eff}$ will be between that for uncoated circuits (previous section) and that for a thickly coated line (see Figure 5-13).

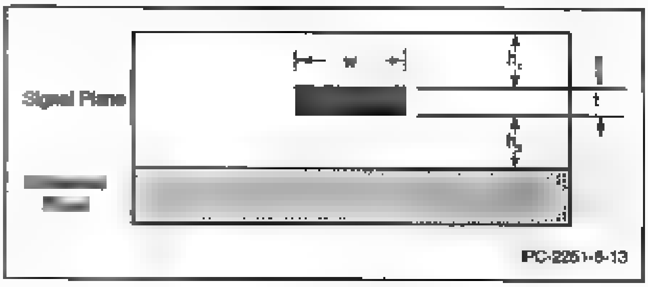


Figure 5-13 Flat Conductor Embedded Microstrip

5.5.2.1 Flat Conductor Embedded Microstrip The following equations give the impedance (Z_0), intrinsic line capacitance (C_0), intrinsic line inductance (L_0), and intrinsic propagation delay (t_{pd}) for embedded microstrip circuitry.

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \times \ln\left(\frac{5.98h_2}{0.8w + t}\right) \times \left(1 \quad \frac{h_1}{0.1}\right) \qquad [0.47]$$

$$t_{pd}\,(\text{ps/in}) = 1000\left(\frac{1.017\sqrt{0.457\,\varepsilon_r + 0.67}}{12\,(\text{in})}\right) \qquad [0.48]$$

$$C_0\,(\text{pF/in}) = \frac{t_{pd}\,(\text{ps/in})}{Z_0\,(\text{ohms})} \qquad [0.49]$$

$$L_0\,(\text{nH/in}) = \frac{[Z_0\,(\text{ohms})]^2\,C_0\,(\text{pF/in})}{1000} \qquad [0.50]$$

restrictions:

Line Widths = 0.127 mm to 0.381 mm
[0.005 in to 0.015 in]
Dielectric Thickness = 0.127 mm to 0.381 mm
[0.005 in to 0.015 in]
Ohms = 40 Ω to 90Ω

where:
h_1 = Dielectric thickness, Signal to Surface
h_2 = Dielectric thickness, Plane to Signal
w = Line width
t = Line thickness

5.5.3 Centered Stripline A centered stripline is a thin, narrow conductor embedded midway between the two AC ground/voltage planes (see Figure 5-14). Since all electric and magnetic field lines are contained between the planes, the stripline configuration has the advantage that EMI will be suppressed except for lines near the edges of the printed circuit board. Because of the presence of ground planes on both sides of a stripline circuit, the capacitance of the line is increased and the impedance is decreased compared to a microstrip line having the same applicable geometries.

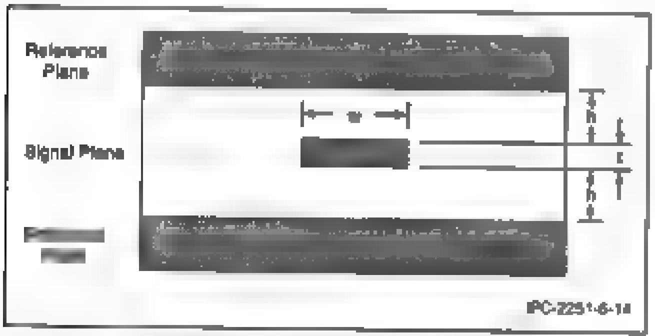


Figure 5-14 Flat Conductor Centered Stripline

5.5.3.1 Wire Centered Stripline Stripline parameters for impedance (Z_0), intrinsic line capacitance (C_0), intrinsic line inductance (L_0), and intrinsic propagation delay (t_{PD}) are presented below for centered wire circuit geometries. The equations assume that the wire is placed midway between the planes (see Figure 5-15).

$$Z_0 = \frac{138}{\sqrt{\varepsilon_r}} \ln\left(\frac{4h}{\pi d}\right) \qquad [0.51]$$

where:
h = Distance between centerline of wire and one ground plane
d = Diameter of wire

5.5.3.2 Flat Conductor Centered Stripline Stripline parameters for impedance (Z_0), intrinsic line capacitance (C_0), intrinsic line inductance (L_0), and intrinsic propagation delay (t_{PD}) are presented below for flat circuit geometries. The equations assume that the circuit layer is placed midway between the planes.

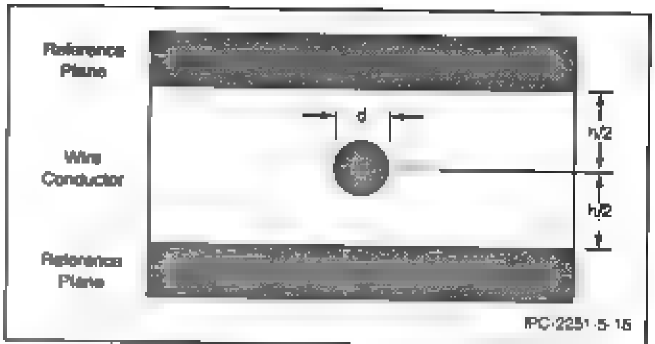


Figure 5-15 Wire Conductor Centered Stripline

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \times \ln\left(\frac{4 \times h}{0.67\pi\,(0.8w + t)}\right) \qquad [0.52]$$

$$t_{pd}\,(\text{ps/in}) = 1000\left(\frac{1.017\,\sqrt{\varepsilon_r}}{12\,(\text{in})}\right) \qquad [0.53]$$

$$C_0\,(\text{pF/in}) = \frac{T_{pd}\,(\text{ps/in})}{Z_0\,(\text{ohms})} \qquad [0.54]$$

$$L_0\,(\text{nH/in}) = \frac{[Z_0\,(\text{ohms})]^2\,C_0\,(\text{pF/in})}{1000} \qquad [0.55]$$

restrictions:

Line Widths = 0.127 mm to 0.381 mm
[0.005 in to 0.015 in]
Dielectric Thickness = 0.127 mm to 0.381 mm
[0.005 in to 0.015 in]
Ohms = 40 Ω to 90Ω

where:
h = Distance between line and reference plane
t = Line Thickness
w = Line Width

5.5.4 Dual-Stripline In the case that a layer of circuitry is placed between two ground (or power) layers, but is not in the middle, the stripline equations must be modified (see Figure 5-16). This is to account for the increased coupling between the circuit and the nearest plane, since this is more significant than the weakened coupling to the distant plane. When the circuit is placed approximately in the middle third of the interplane region, the error caused by assuming the circuit to be centered will be quite small.

An asymmetric transmission line closely approximates a stripline except that the signal line is offset from the centerline between the power planes. The circuits on one layer are generally orthogonal to those on the other to keep parallelism and crosstalk between layers to a minimum.

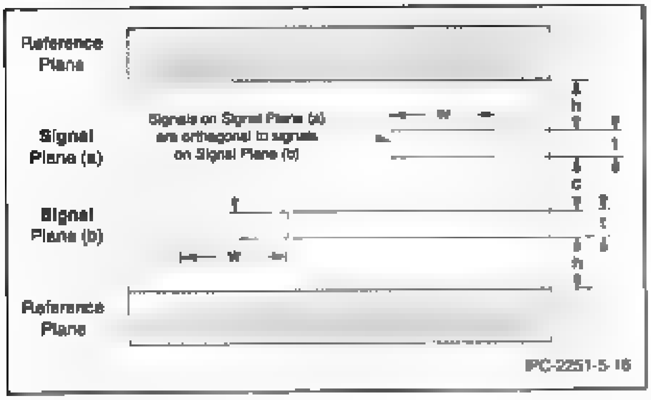


Figure 5-16 Flat Conductor Dual Stripline (Asymmetrical Signals

5.5.4.1 Flat Conductor Dual Stripline (Asymmetric Signals) The impedance Z_0, intrinsic line capacitance C_0, intrinsic line inductance L_0, and intrinsic propagation delay (t_{pd}) are presented below.

$$Z_0\ (\text{ohms}) = \frac{A+B}{2} \qquad [0.56]$$

$$A\ (\text{ohms}) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{8h}{0.67\pi\,(0.8w+t)}\right)$$

$$B\ (\text{ohms}) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{8\,(h+c)}{0.67\pi\,(0.8w+t)}\right)$$

$$t_{pd}\ (\text{ps/in}) = 1000\left(\frac{1.017\sqrt{\varepsilon_r}}{12\ (\text{in})}\right) \qquad [0.57]$$

$$C_0\ (\text{pF/in}) = \frac{t_{pd}\ (\text{ps/in})}{Z_0\ (\text{ohms})} \qquad [0.58]$$

$$L_0\ (\text{nH/in}) = \frac{(Z_0\ (\text{ohms}))^2\, C_0\ (\text{pF/in})}{1000} \qquad [0.59]$$

where:

h = Distance, signal to nearest plane
c = Signal plane separation
t = Line thickness
w = Line width

Restrictions:

Line Widths = 0.127 mm to 0.381 mm
[0.005 in to 0.015 in]
Dielectric Thickness = 0.127 mm to 0.381 mm
[0.005 in to 0.015 in]
Ohms = 40 Ω to 90Ω

This stackup is shown in Figure 5-16. As with stripline, EMI will be shielded except for signal lines near the edges of the AC ground planes. The two signal layers do not electrically interact with each other. This is usually accomplished by making them orthogonal.

5.5.5 Differential Pair Conductors Differential pair conductors are deliberately routed to produce desired coupled impedance. This impedance is generally line-to-line. There are many types of differential pairs but all are generally grouped into two categories. Those categories are Broad-Side Coupled and Edge Coupled.

5.5.5.1 Broadside Coupled Wires The differential (or odd mode) stripline impedance Z_0, for Figure 5-17, is presented below.

$$Z_0 = \frac{276}{\sqrt{\varepsilon_r}}\left(\log_{10}\left(4h\,\frac{\tanh\left(\frac{\pi s}{2h}\right)}{\pi d}\right)\right) \qquad [0.60]$$

where:

H = Plane separation
d = Wire diameter
s = Wire center-center spacing

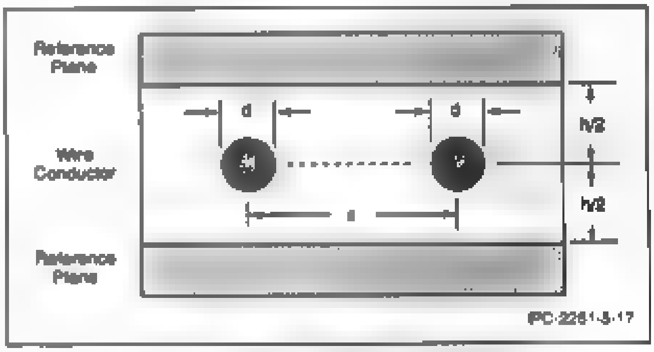


Figure 5-17 Wire Conductor Differential Centered Stripline

Broadside-Coupled differential pairs are typically (but not always) routed on adjacent layers. The coupled impedance is created from the field that couples between the flat (broad sides) of the conductors.

Edge Coupled differential pairs are generally routed on the same layer. The coupled impedance is created from the field between the edges of the conductors.

5.5.5.2 Broadside Coupled Differential Stripline This is also called a differential pair. In this case, two directly coupled (broad-side coupled) conductors are routed in adjacent layers. The mutual coupling between the conductors create differential line-to-line impedance and is dependent upon conductor width and dielectric layer thickness. Also present, is the line-to-ground impedance created by dielectric layer spacing to the closest AC reference planes. Both line-to-ground and line-to-line spacing determines the differential impedance of the pair.

5.5.5.2.1 Broadside Coupled Flat Conductor Shielded Differential Stripline Differential stripline impedance Z_0 is presented below. See Figure 5-18 for Flat Conductor Shielded Broadside Coupled Differential Stripline and 5.5.5.2.2 for Flat Conductor Shielded Edge Coupled Differential Stripline.

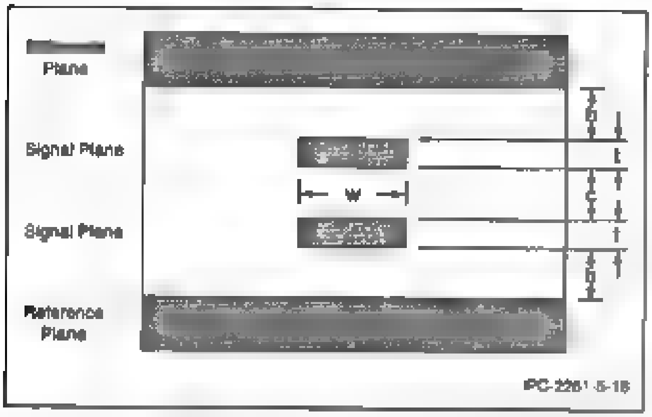

Plane
Signal Plane
w
Signal Plane
Reference Plane
h
t
c
t
h
IPC-2251-5-18

Figure 5-18 Flat Conductor Shielded Broadside Coupled Differential Stripline

$$Z_0 = \frac{82.2}{\sqrt{\varepsilon_r}}\left(\ln\left(\frac{5.98c}{0.8w+t}\right)\right)\left(1-e^{-0.6h}\right) \qquad [0.61]$$

5.5.5.2.2 Flat Conductor Nonshielded Broadside Coupled Differential Stripline Removing the shield planes cause the value of 'h' to become very large. See Figure 5-19 for Nonshielded Broadside Coupled Differential Stripline.

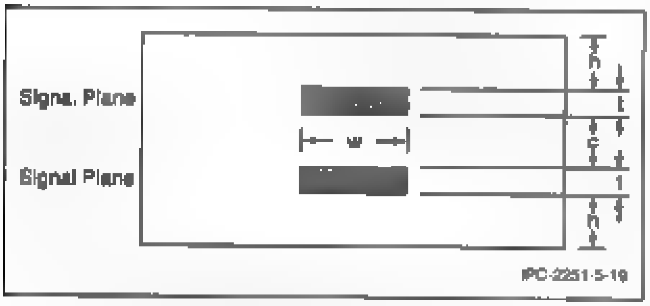

Signal Plane
w
Signal Plane
h
t
c
t
h
IPC-2251-5-19

Figure 5-19 Flat Conductor Nonshielded Broadside Coupled Differential Stripline

Substituting a value of 100 or greater for 'h' has the same effect as eliminating the last term in Equation [0.61] Thus the differential Impedance is determined using the following Equation.

$$Z_0 = \frac{82.2}{\sqrt{\varepsilon_r}}\ln\left(\frac{5.98c}{0.8w+t}\right) \qquad [0.62]$$

5.5.5.3 Edge Coupled Differential Stripline This is also called a differential pair. In this case, two directly Edge (Side-by Side) coupled conductors are routed on the same layer. The mutual coupling between the conductors creates differential line-to-line impedance and is dependent upon conductor width and dielectric layer thickness Also present, is the line-to-ground impedance created by dielectric layer spacing to the closest AC reference planes. Both line-to-ground and line-to-line spacing determines the differential impedance of the pair (see Figures 5-20 and 5-21). Note that in the Flat Conductor Shielded Edge coupled Differential Dual Stripline model, Figure 5-21, the differential pair traces could be located in signal plane (a), signal plane (b), or both.

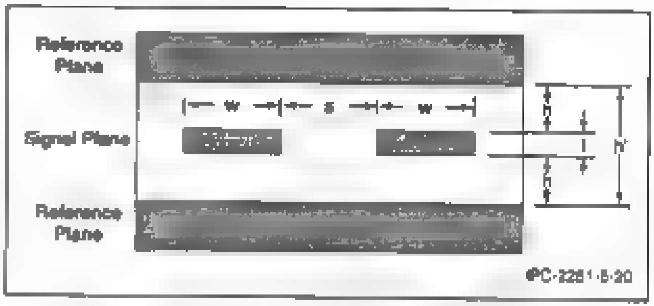

Reference Plane
w
s
w
Signal Plane
Reference Plane
h
t
h
h'
IPC-2251-5-20

Figure 5-20 Flat Conductor Shielded Edge Coupled Differential Stripline

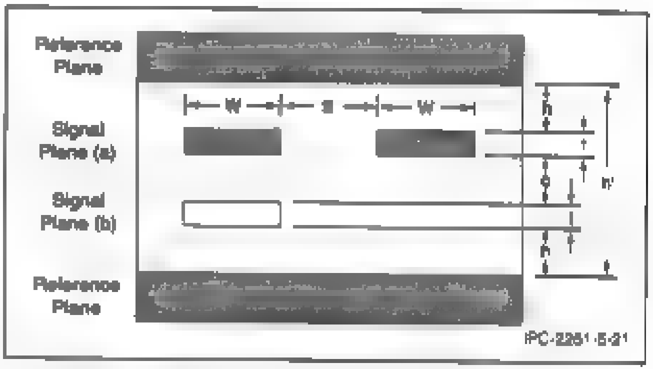

Reference Plane
w
s
w
Signal Plane (a)
Signal Plane (b)
Reference Plane
h
t
c
t
h
h'
IPC-2251-5-21

Figure 5-21 Flat Conductor Shielded Edge Coupled Differential Dual Stripline

$$Z_{diff,stripline}\,(\text{ohms}) = 2Z_0\left(1-0.374e^{\left(-2.9\frac{s}{h}\right)}\right) \qquad [0.63]$$

where:

$h' = 2h + t$
Z_0 is given in [5.54]
t_{pd} is given in [5.55]
C_0 is given in [5.56]
L_0 is given in [5.57]

$$Z_{diff,stripline} = [0.63]$$

where:

$h' = 2h + 2t + c$
Z_0 is given in [5.58]
t_{pd} is given in [5.59]
C_0 is given in [5.60]
L_0 is given in [5.61]

5.5.5.4 Edge Coupled Differential Microstrip Differential microstrip impedance Z_0 as shown in Figures 5-22 and 5-23, is presented below.

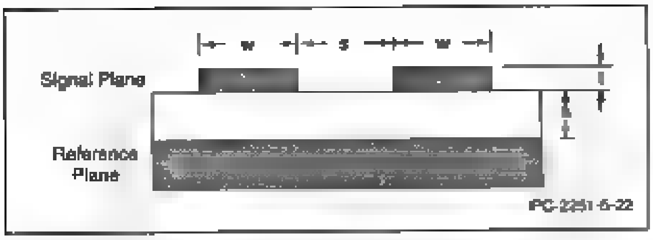


Figure 5-22 Flat Conductor Edge Coupled Differential Surface Microstrip

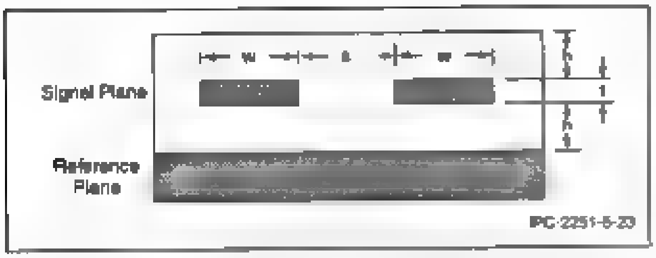


Figure 5-23 Flat Conductor Edge Coupled Differential Embedded Microstrip

$$Z_{diff,microstrip}\ (ohms) = 2Z_0\left(1 - 0.48e^{\left(-0.96\frac{s}{h'}\right)}\right) \qquad [0.64]$$

where:

$h' = h$
Z_0 is given in [5.42]
t_{pd} is given in [5.43]
C_0 is given in [5.45]
L_0 is given in [5.46]

$$Z_{diff,microstrip} = [0.64]$$

where:

$h' = 2h + t$
Z_0 is given in [5.47]
t_{pd} is given in [5.50]
C_0 is given in [5.51]
L_0 is given in [5.52]

5.6 Loading Effects Signal lines are subdivided into logical interconnect and physical interconnect models. The logical interconnect models define the function of the signal line. The physical interconnect models define physical connectivity of the logic models. The classification for interconnect models is shown in Table 5-5.

Table 5-5 Logic Model Classifications

Logical	Physical
> NET	1) Capacitive 2) Transmission line
> BUS	1) Distributed 2) Lumped
> WIRED-AND/OR	1) Radial

A Net consists of a single source and one or more destinations. A Bus consists of multiple sources and one or more destinations with only one source active at any given time. A Wired-AND consists of multiple sources and one or more destinations with multiple sources active at any given time. These logical configurations will be developed further in 5.6.5.

5.6.1 Termination Resistors Termination resistors perform two basic functions. The first is to minimize signal reflections caused by a mismatch between the last signal load and the loaded transmission line impedance. Resistors are put in parallel with the load input to match the impedance.

The second method is used with heavily loaded transmission lines. This method uses series resistors. These resistors are connected between the source and the conductor. These resistors slow the rise time of the signal such that reflections will not occur.

5.6.2 Reflections In a transmission line environment, the signal is actually an electromagnetic energy pulse. When the signal travels down the signal line, of impedance Z_0, and reaches a load or line segment of the same impedance, it transfers the entire energy onto it.

If the impedance of the load, Z_L, is different, a percentage of the energy pulse is transmitted onto the load and the balance is returned (reflected) back towards the source. The reflected amount can be calculated using a resistive voltage divider concept.

The percent of voltage reflected back towards the source is shown by the load reflection coefficient, ρ_L where,

$$\rho_L = \frac{(Z_L - Z_0)}{(Z_L + Z_0)} \qquad [0.65]$$

The above also holds for the source. If the source impedance differs from the transmission line a percentage of the reflected energy will be reflected back towards the load. The source reflection coefficient, ρ_S

$$\rho_s = \frac{(Z_S - Z_0)}{(Z_S + Z_0)} \qquad [0.66]$$

5.6.3 Minimum Separation Before a definition of the signal line classifications is presented, the concept of minimum load separation is required. This is required because the signal environment definition difference between a lumped load and a distributively loaded transmission line environment is dependent on the spacing at which loads start to affect each other. The minimum load separation distance defines the point at which the reflections from a load on a transmission line begin to affect adjacent loads. In this section a pulse is assumed to have a linear ramp edge transition rate. Exponential rounding at the beginning and end of the transition can be neglected.

In a circuit board environment, a logic input has an effective capacitance associated with it. In a transmission line, whenever a capacitive load is attached to the line a point discontinuity occurs. Each of these discontinuities will pass a majority of the incident pulse down the line and a portion of the incident pulse will be reflected back towards the source. The width of the reflected pulse is a function of the edge transition rate of the incident pulse.

To isolate the effects of this capacitive load on previous loads there must be a minimum separation distance, LSEP, maintained between adjacent loads such that the reflected pulses will not add up sufficiently to detract from the continuity of the signal. L_{SEP} is calculated in the following manner:

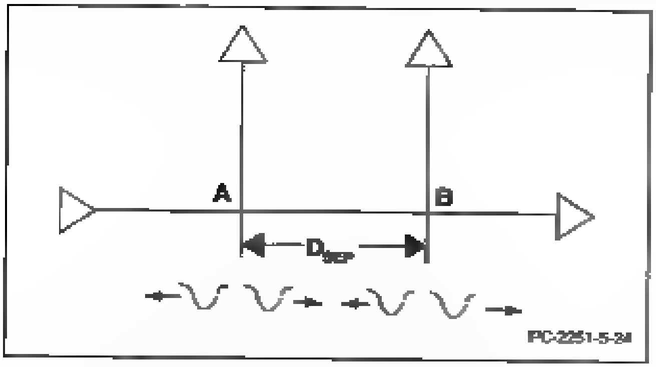


Figure 5-24 Net Illustrating Point Discontinuity Waveforms

The reflected pulse width is directly equal to the propagation time between points A and B. The two-way propagation time between points A and B in Figure 5-24 is:

$$T_{WA} = 2\,(D_{SEP})\,(t_{pd}) \qquad [0.67]$$

where,

T_{WA} = Width of reflected pulse from A
D_{SEP} = Distance between A and B
t_{pd} = Unloaded line propagation delay

The reflected pulse width, T_{WA}, is expressed by,

$$T_{WA} = 1.7\,(t_r) \qquad [0.68]$$

where, t_r = 10%-90% Edge transition rate

Combining equations [0.67] and [0.68] yields.

$$1.7\,(t_r) = 2\,(D_{SEP})\,(t_{pd}) \qquad [0.69]$$

$$D_{SEP} = \frac{(1.7t_r)}{(2t_{pd})} \qquad [0.70]$$

$$D_{SEP} = \frac{0.85t_r}{t_{pd}} \qquad [0.71]$$

For a 74Sxx edge transition time of 3.0 nsec and a FR-4 microstrip line propagation time of t_{pd} = 0.148 ns/in.,

$$D_{SEP} = 0.85\left(\frac{3.0}{0.148}\right) = 17.2\text{ in.} \qquad [0.72]$$

Equation [0.72] shows that if the reflected pulse from point B is to have no interaction with point A the loads must be separated by 437 mm [17.2 in]. This distance between loads is the minimum distance between loads to prevent reflections from overlapping. If the pulses are allowed to overlap and the maximum overlap of the two pulses is limited so the maximum amplitude will be less than the maximum amplitude of either pulse, the minimum separation distance can be reduced without affecting the worst-case results. This can be extended to calculate the minimum separation between adjacent loads such that the additions of the reflections from adjacent discontinuities do not exceed the maximum amplitude of either pulse.

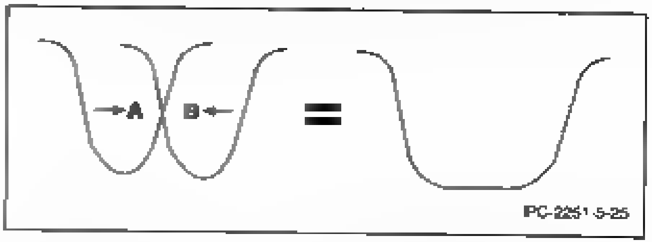


Figure 5-25 Addition of Two Pulses Traveling Opposite Directions

As shown in Figure 5-25 the addition of the two pulses reaches the maximum amplitude and width when one-half of the pulse from A coincides with one-half of the pulse from point B (assuming the load characteristics of point A are equal to point B). Using equations [0.68] for an overlap of 1/2 the pulse width, equation [0.70] becomes:

$$D_{SEP\,0.5\,overlap} = 0.5\,(0.85)\,\frac{t_r}{t_{pd}} \qquad [0.73]$$

$$= 0.425\,\frac{t_r}{t_{pd}}$$

For, t_r = 3.0 ns and t_{pd} = 0.148 ns/in. and using equation [0.73]

$$D_{SEP\,0.5\,overlap} = 0.425\left(\frac{3.0}{0.148}\right) = 8.6\text{ in.} \qquad [0.74]$$

Equation [0.74] shows that if the loads are separated by more than 218 mm [8.6 in] for 74Sxx devices, a LOADED transmission line environment will not exist. The effective transmission line impedance will not be affected. The capacitive loads will generate noncoherent pulses on the transmission line.

Edge transition times, thus propagation times, will be affected due to the energy loss as the pulse travels by each capacitive load.

The following sections assume that loads are connected at intervals less than the minimum separation distance unless otherwise specified.

5.6.4 Distributed Loading A distributively loaded line is a transmission line where the separation between loads or load clusters is less than the minimum separation distance, equation [0.70]. The loads can be evenly or unevenly distributed along the line (see Figure 5-26).

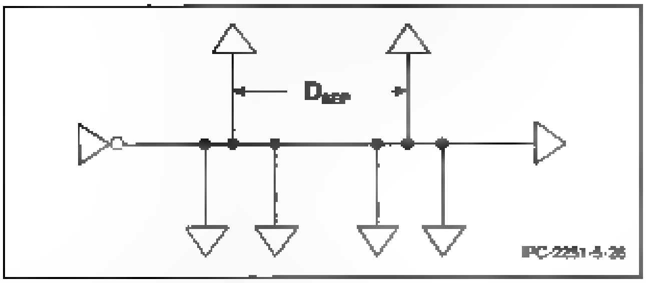


Figure 5-26 Distributed Line

The transmission line lumped element model simulates the line as a series inductor and parallel capacitor. Each load is treated as a capacitor for AC analysis. The load input resistance is usually neglected due to its high value relative to the line impedance.

Main line is defined to be the conductor between the source and the furthest load. The length of the main line will be the signal line length. All loads that attach in-between the source and furthest load are connected with a line called stubs. As stated above, if the stub length meets the requirements the inherent capacitance of the stub must be included as part of the load capacitance.

When the loads are distributed along the transmission line the effective capacitance per unit length is increased. This will affect the propagation delay and line impedance as follows.

$$C_L = N\,C_{in} \qquad [0.75]$$

$$C_D = D_M C_0 \qquad [0.76]$$

$$Z_0 = \sqrt{\left[\frac{L_D}{(C_D + C_L)}\right]} \qquad [0.77]$$

$$Z'_0 = \sqrt{\left(\frac{L_D}{C_D}\right)}\left(\sqrt{\frac{1}{1 + \frac{C_L}{C_D}}}\right) \qquad [0.78]$$

Simplifying Equation [0.78], we get:

$$Z'_0 = \frac{Z_0}{\sqrt{\left(1 + \frac{C_L}{C_D}\right)}} \qquad [0.79]$$

where:

C_L = Total load capacitance
C_D = Total line capacitance
Z_O = Loaded line impedance
N = number of loads
C_{IN} = Single load capacitance
D_M = Main line length
L_D = Total line inductance
C_O = Line capacitance per unit length
Z'_O = Effective line impedance

$$t_{pdL} = t_{pd}\sqrt{\left(1 + \frac{C_L}{C_D}\right)} \qquad [0.80]$$

where, t_{pd} = Propagation delay-time per unit-length

Each load connection to the main line should have a stub less than 1/4 of the minimum separation distance. This will minimize the noise on the main line. The length and inherent capacitance of the stub must be included as part of the load capacitance value used for C_{IN} and C_L in the above equations.

Example: Consider a microstrip line with loads that are distributively attached. Stub lengths = 0 in.

D_M = 10.0 inch
C_O = 2.0 pf/in
C_{IN} = 5.0 pf
Z_O = 50 ohms
t_{pd} = 0.148 ns/in
N = 6 loads

From equation [0.75],

C_L = 6 (5pF) = 30 pF

From equation [0.76],

C_D = 10 in (2pF/in) = 20 pF

From equation [0.79],

$$Z_0 = \frac{50}{\sqrt{\left(1 + \frac{30}{20}\right)}} = 31.6 \text{ ohms}$$

And from equation [0.80],

$$t_{pdL} = 0.148\left(\sqrt{1 + \frac{30}{20}}\right) = 0.234 \text{ ns/in}$$

Where t_{pdL} = propagation delay due to capacitive loading.

As shown in this example the loading can greatly influence the final loaded line impedance. In some instances minimum loaded line impedance is required to keep the first signal plateau beyond required threshold value.

N/D_M is called the maximum loading density. This value will yield the maximum loads per unit length that will maintain Z_O above the minimum predefined value.

$$\frac{N}{D_M} = \frac{C_0}{C_L}\left[\left(\frac{Z_0}{Z'_0}\right)^2 \quad 1\right] \qquad [0.81]$$

5.6.5 Lumped Loading A lumped loaded line is a transmission line whose separation between loads is greater than the minimum separation distance, equation [0.70] (see Figure 5-27). A transmission line environment disappears when lines become heavily loaded near the source causing the signal edge transition time to increase. A lumped load may be a single load or a cluster of loads at any given point.

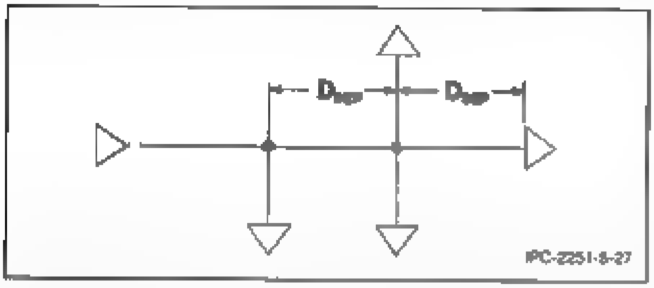


Figure 5-27 Lumped Loading

A load cluster (see Figure 5-28) consists of multiple loads that are connected to the same point by stubs (star configuration), or a section of the line where several loads are connected as distributed loads.

Lumped loads configured as short distributed lines behave as discontinuities to the transmission line. A series of loads that are within the minimum separation distance will create a distributively loaded transmission line, Z_O. If this section of the transmission line has a length less than $t_r/(2t_{pd})$, the loads will be treated as a lumped capacitive load.

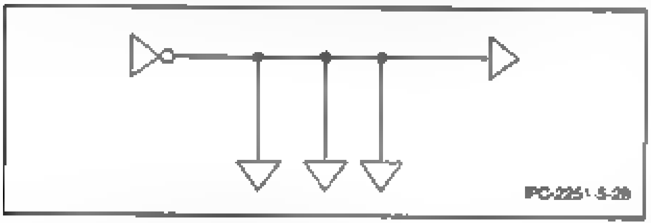


Figure 5-28 Short Distributively Loaded Cluster

If the length is greater than $t_r/(2t_{pd})$, the section will be treated as a distributed line and the propagation characteristics will be handled as such.

A TTL/MOS load is modeled as a capacitive load. This capacitive load presents a point discontinuity to the transmission line. The load is modeled as a Thevinin equivalent capacitor and resistor as shown in Figure 5-29.

Since the reflections from each point load are not additive, the propagation delay will not be affected except for energy losses that occur as the waveform passes. Reflections will show up as glitches in the waveform, as shown in Figure 5-30 and will have a magnitude of:

$$V_R = \frac{C_L\,(Z_0)\,(V_A)}{(2t_r)} \qquad [0.82]$$

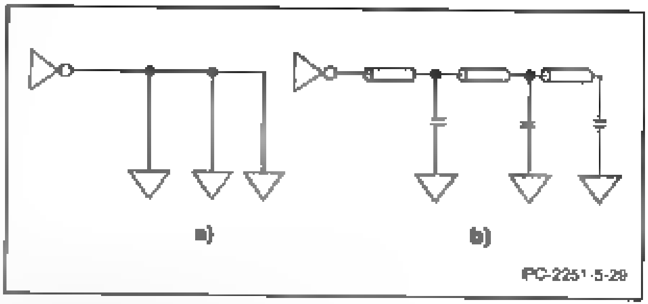


Figure 5-29 a) Lumped Loaded Transmission Line b) Equivalent Model

where:

V_R = Reflected voltage
C_L = Node capacitance
Z_O = Line impedance
V_A = Incident pulse amplitude
t_r = Edge transition time

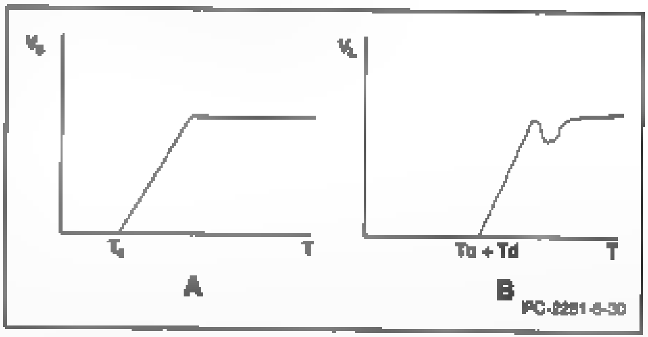


Figure 5-30 Waveforms for a Lumped Capacitive Load

Additional propagation delay is injected as a result of the time constant, T_{DL}, of the load. For loads whose equivalent resistance, R_L, cannot be neglected equation [0.83] presents its effect on the edge transition rate.

$$T_{DL} = \frac{R_L Z_0 C_L}{R_L + Z_0} \qquad [0.83]$$

If there is not termination resistance or $R_L >> Z_o$ the additional propagation delay is,

$$T_{DL} = Z_0 C_L \qquad [0.84]$$

Equation [0.82] will be used as a first order approximation for timing analyses.

Example:

Microstrip transmission line is lumped loaded at end with six loads (see Figure 5-31).

D_M = 10.0 inch
Z_O = 50 ohms
C_O = 2.0 pf/in
T_{PD} = 0.148 ns/in
C_{IN} = 5.0 pf
N = 6 loads
R_L = 10K

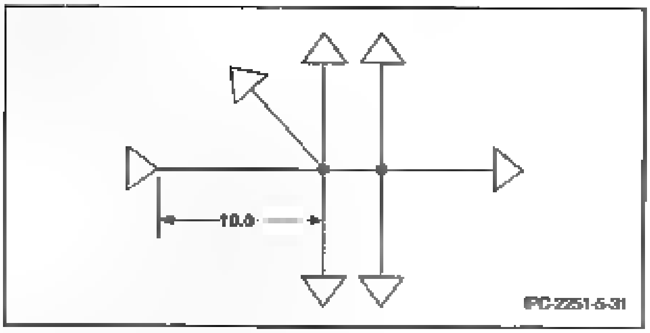


Figure 5-31 Lumped Transmission Line

From equation [0.75],

$$C_L = 6\,(5\text{ pF}) = 30\text{ pF}$$

From equation [0.79],

$$Z'_0 = \frac{50}{\sqrt{\left[1 + \frac{30}{10\,(2)}\right]}} = 31.6\text{ ohms}$$

From equation [0.80],

$$t_{pdL} = 10\,(0.148\text{ ns}) = 1.48\text{ ns}$$

From equation [0.83],

$$T_{DL} \quad \frac{10^4\,(31.6)\,(30 \times 10^{-12})}{10^4}$$

$$T_{DL} = 946\text{ ps}$$

From equation [0.84],

$$T_{DL} = 31.6\,(30 \times 10^{-12}) = 946\text{ ps}$$

$$T_{D\,Line} = t_{pd} + T_{DL} \qquad [0.85]$$

$$T_{D\,Line} = 1.48\text{ ns} + 946\text{ ps} = 2.43\text{ ns}$$

5.6.6 Radial Loading A radial load is a stub of sufficient length and loading that generates a pulse greater than the noise budget and affects the input of another load. The worst-case interference will be when a load is located at the junction of the radial line to the main line.

Radial loading occurs when multiple lines diverge from a common point on a line. The divergence point can be located at the source output or at any point along the transmission line, as shown in Figure 5-32.

As defined above, radial loading occurs when multiple lines diverge from a common point on the main line. Each of these lines has a length greater than the minimum separation distance. Each radial line can be individually treated as a distributed, lumped, or unloaded transmission line dependent on its loading characteristics.

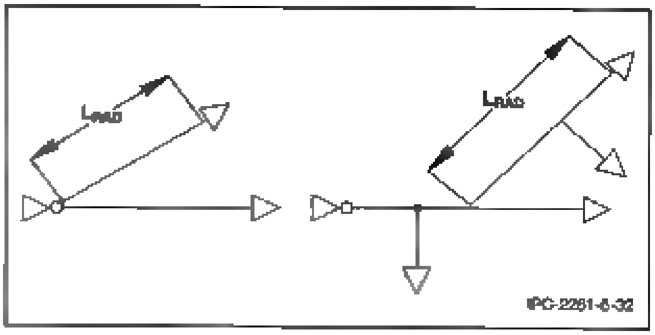


Figure 5-32 Radial Loading

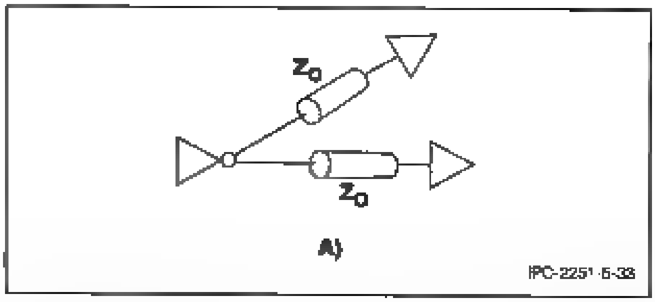


Figure 5-33 Example Configuration

As shown in Figure 5-33, when a pulse is propagating down a transmission line equal to Z_O and it hits a radial line contact point the effective impedance at that point is $Z_O/2$ (assuming each radial line has an impedance equal to Z_O and there are two radial lines as shown in Figure 5-33). If the impedance of the main line and the radial line are equal the pulse will split evenly and 1/3 will travel down each line, and 1/3 is reflected back towards the driver.

Radial lines affect the propagation characteristics of the transmission line by creating the impedance Z_{RAD} at that point. Where,

$$Z_{RAD} = \frac{Z_0}{N} \qquad [0.86]$$

where, N = Number of radial lines

Each incidence of a radial line will divide the pulse even further. Rules governing system layout must limit the number of radial lines on any given signal line to two. This, coupled with distributed loading effects of the radial and main line will maintain a manageable transmission line environment.

The propagation time for a radial line will be mostly affected by the interaction of the radial line and the main line (see Figure 5-34). Recall that for the main line, Dm is the distance between the driver and the farthest load. If the net impedance of the intersection results in the signal to drop below threshold for a Low-to-High transition or rise above threshold on a High-to-Low transition, the signal line timing will be affected.

The most prevalent implementation of a radial line structure is that of a multiple driver signal line.

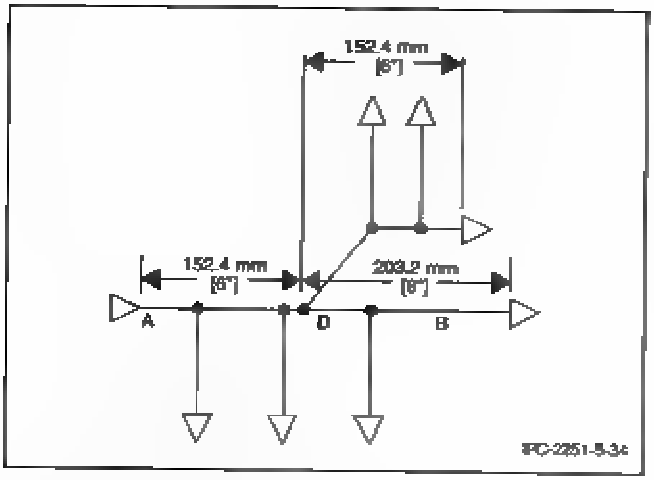


Figure 5-34 Example of Radial Line

Example:

Microstrip transmission line, distributively loaded

$D_M = 14.0$ in
$C_O = 2.0$ pf/in
$C_{IN} = 5.0$ pf
$D_{RAD} = 6$ in
$t_{pd} = 0.148$ ns/in
$Z_O = 50$ ohms

$C_{L,\ main}$ = 4 branches (5 pF/branch) = 20 pF

$C_{D,\ main}$ = 14 in (2 pf/in) = 28 pF

$C_{L,\ radial}$ = 3 branches (5 pF/branch) = 15 pF

$C_{0,\ radial}$ = 6 in (2 pF/in) = 12 pF.

From equation [0.78],

$$Z'_{0,\ main} \quad \frac{50}{\sqrt{\left(1+\frac{20}{28}\right)}} \quad 38.2 \text{ ohms}$$

$$Z'_{0,\ radial} \quad \frac{50}{\sqrt{\left(1+\frac{15}{12}\right)}} \quad 33.3 \text{ ohms}$$

At point D the impedance is:

$$Z'_{0,\ parallel} = \frac{(33.3+38.2)}{33.3\,(38.2)} = 17.8 \text{ ohms}$$

From equation [0.80],

$$t_{pd,\ main} = 0.148\sqrt{\left(1+\frac{20}{28}\right)} = 0.194 \text{ ns/in}$$

$$t_{pd,\ radial} = 0.148\sqrt{\left(1+\frac{15}{12}\right)} = 0.222 \text{ ns/in}$$

Thus,

$$T_{D,\ A\text{-}B} = 14\,(0.194) = 2.72 \text{ ns}$$

$$T_{D,\ A\text{-}D} = 6\,(0.194) + 6\,(0.222) = 2.5 \text{ ns}$$

5.6.7 Logic Signal Line Loading Models

5.6.7.1 Net A net is a single source multiple destination signal line, Figure 5-35. Timing analysis is performed dependent on the load configuration of the net.

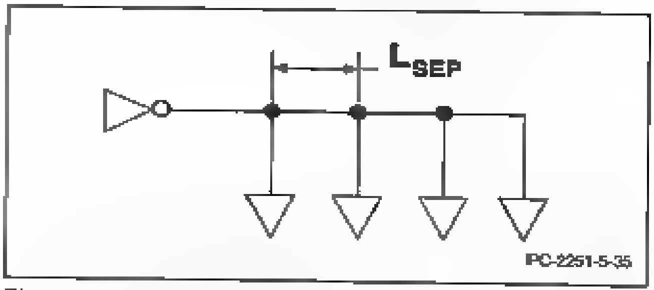


Figure 5-35 Net Configuration

5.6.7.2 Bus A bus is a multiple source multiple destination signal line, as shown in Figure 5-36. Only one source may be active at any point in time. The sources may be a combination of tri-state and open-collector devices.

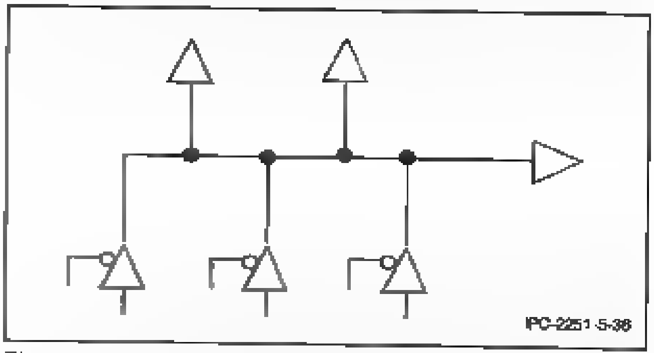


Figure 5-36 Bus Configuration

For timing analyses, all of the physical configurations must be analyzed. The first analysis involves the distributed line analysis.

Termination resistors must be attached to the bus based on the results of the above analyses. Due to the complexity of resistor placement the procedure for termination placement will not be analyzed. It is sufficient to state that the resistors should be placed at locations that will reduce the load impedance such that unwanted reflections and back-porching will be limited.

5.6.7.3 Wired - AND/Wired - OR The wired-AND and wired-OR configuration, Figure 5-37, is a multiple source multiple destination bus which can have greater than one source active at a given point in time. Sources connected to the line must have open-collector output structures with a pull-up/termination resistor network.

Use of wired-AND and wired-OR circuit configurations is nonpreferred and should be avoided if possible. Use of a

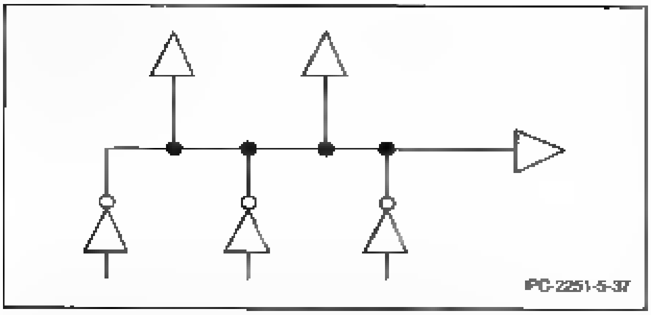


Figure 5-37 Wired-AND Configuration

multiple source, multiple destination bus with the potential for more than one source to be simultaneously active complicates fault-isolation and repair operations significantly.

5.6.6 Timing Calculation This section presents two commonly used models for determination timing effects of a loaded transmission line on the output of the driving impetus.

5.6.6.1 Bergeron Plot The graphical method of finding the transients in a transmission line terminated by nonlinear resistances originates from Bergeron. Its use is illustrated here on a transmission line interconnecting two TTL inverters as shown in Figure 5-38a.

In Figure 5-38a, the output of a TTL inverter is connected to the input of a second one by a transmission line with a characteristic impedance of $Z_O = 50$ ohms and a propagation delay of T_O. Typical voltage-current characteristics of the TTL inverters are shown in Figure 5-38b. When the output of the first inverter is logic 0, the static operating point is given by the intersection of the V_{out} vs I_{out} for logic 0 output curve with the V_{in} vs I_{in} curve, and is marked as point "0." Similarly, when the output of the first inverter is logic 1, the static operating point is given by the intersection of the V_{out} vs I_{out} for logic 1 output curve with the V_{in} vs I_{in} curve, and is marked as point "1."

We first find the transients for the case when the output of the first inverter changes from logic 0 to logic 1 at time t = 0. For times t < 0, V_{out}, V_{in}, I_{out}, and I_{in} are given by point "0" in Figure 5-38b. At time t = 0, the output of the first inverter changes to logic 1 and as a result V_{out} and I_{out} instantaneously move from point "0" to somewhere onto the V_{out} and I_{out} curve. Hence V_{out} and I_{out} will each change by some amount. We designate these changes by ΔV_{out} and ΔI_{out}, respectively. The output of the first inverter is connected to the left end of the transmission line, thus a signal characterized by ΔV_{out} and ΔI_{out} starts traveling to the right. However, for a signal traveling to the right the ratio of the change in voltage to the change in current is Z_O, that is, $\Delta V_{out}/\Delta I_{out} = Z_O$. This relation now constrains the new point of V_{out} and I_{out} on the V_{out} vs I_{out} for logic 1 output curve to be in a direction with respect to point "0" such that $\Delta V_{out}/\Delta I_{out} = ZO = 50$ ohms. This constraint is satisfied by a straight line with a slope of 50 ohms drawn through point "0." Thus, the intersection of this straight line with the V_{out} vs I_{out} for logic 1 output curve, shown as point A in Figure 5-38c, determines V_{out} and I_{out} for times $0 < , t < 2T_O$.

The signal that is traveling to the right and that is characterized by a change from point "0" to point A in Figure 5-38c reaches the right end of the transmission line at time $t = T_O$. As a result, at time $t = T_O$, VIN and I_{in} will move from point "0" to another point somewhere onto the V_{in} vs I_{in} curve. V_{in} and I_{in} at this point, which we denote point B, are each composed of three constituents, the initial conditions given by point "0," the incident signal given by ΔV_{out} and ΔI_{out}, and a reflected signal that we characterize by ΔV_{in} and ΔI_{in}. The sum of the initial conditions given by point "0" and of the incident signal given by ΔV_{out} and ΔI_{out} is represented by point A. Thus, the difference between point B and point A represents the reflected signal, which is characterized by $\Delta V_{in}/\Delta I_{in} = -Z_o = -50$ ohms. Hence, point B can be found as the intersection of the V_{in} vs I_{in} curve with a straight line that originates from point A and that has a slope of -50 ohms (see Figure 5-38c).

The reflected signal characterized by ΔV_{in} and ΔI_{in} reaches the left end of the transmission line at time $t = 2T_o$ and will change V_{out} and I_{out} from point B to some other point on the V_{out} vs I_{out} for logic 1 output curve: We designate this new point as point C. By using reasoning similar to that above, we can show that point c can be found as the intersection of the V_{out} vs I_{out} for logic 1 output curve with a straight line that originates from point B and that has a slope of 50 ohms. The process may also be continued to obtain additional points, as shown in Figure 5-38c for points D, E, and F. Figure 5-38c also indicates that as the number of points is increased, they approach the final static operating point, point "1," as expected.

The diagram of Figure 5-38c contains all information required for plotting V_{out}, I_{out}, V_{in} and I_{in} as functions of time. The output of the first TTL inverter changes from logic 0 to logic 1 at time t = 0, hence, V_{out} and I_{out} change from their initial values given by point "0" to the values given by point A at time t = 0. The projection of point "0" onto the vertical axis provides the initial value of V_{out} (t < 0) = 0.15 V, and the projection of point "0" onto the horizontal axis provides the initial value of I_{out} (t < 0) = -1.5 mA.

Continuing the reference to Figure 5-38d, for times $0 < t < 2T_O$, the projection of point A onto the vertical axis provides V_{out} $(0 < t < 2T_O) = 1.3$ V, and the projection of point A onto the horizontal axis provides I_{out} $(0 < 2 < T_O) = 22$ mA. Further values of V_{out} and I_{out} can be similarly found from points C and E as shown in the left two graphs of Figure 5-38d.

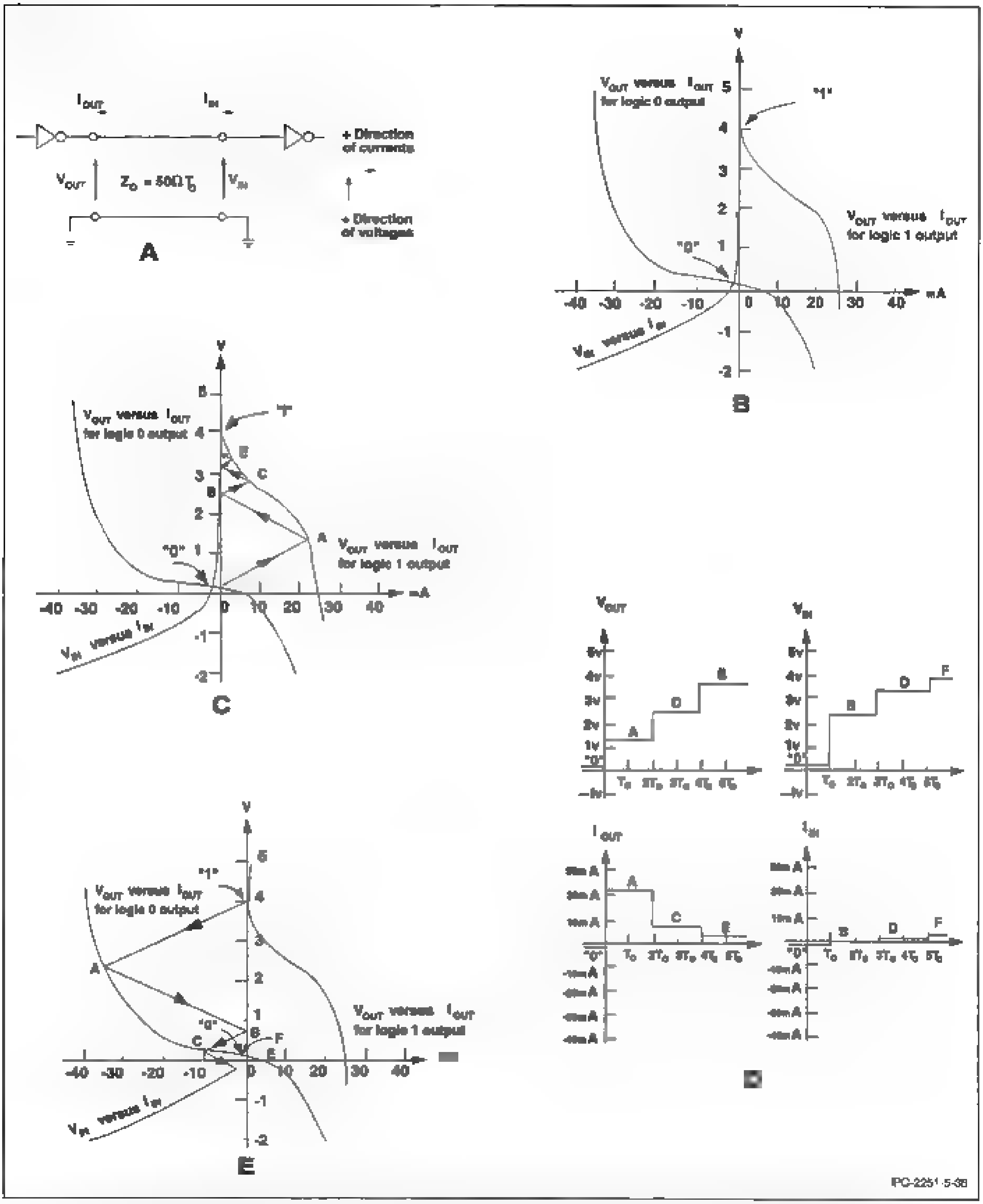

I_OUT
I_IN
+ Direction of currents
V_OUT
Z_0 = 50Ω T_0
V_IN
+ Direction of voltages
A
V
V_OUT versus I_OUT for logic 0 output
"1"
V_OUT versus I_OUT for logic 1 output
"0"
mA
V_IN versus I_IN
B
C
A
B
C
E
D
E
F
V_OUT
V_IN
I_OUT
I_IN
5v
4v
3v
2v
1v
-1v
T_0
2T_0
3T_0
4T_0
5T_0
30m A
20m A
10m A
-10m A
-20m A
-30m A
-40m A
IPC-2251-5-38

Figure 5-38 Multiple Reflections In A Transmission Line Between Two TTL Inverters. (a) The circuit; (b) typical static characteristics of the TTL inverters; (c) transition from logic 0 to logic 1 in the voltage-current plane; (d) V_{out}, I_{out}, V_{in}, and I_{in} as functions of time for a transition from logic 0 to logic 1; (e) transition from logic 1 to logic 0 in the voltage-current plane; (f) V_{out}, I_{out}, V_{in}, and I_{in} as functions of time for a transition from logic 1 to logic 0.

Referring to the right 2 graphs of Figure 5-38d, at the right end of the transmission line, V_{in} and I_{in} remain at their values given by point "0" until Time t = T_O, that is, V_{in} (t= 0.15 V and I_{in}(t T_O) = 1.5 mA. For times $T_O < t < 3T_O$, the values of V_{in} and I_{in} are given by the projections of point B as $V_{in}(T_O < t < 3T_O)$= 2.35 V and I_{in} $(T_O < t < 3T_O)$ = 0.5 mA. Further values of V_{in} and I_{in} are obtained from points D and F and are shown in the right two graphs of Figure 5-38d.

The transients in the circuit of Figure 5-38a were determined in Figure 5-38c and Figure 5-38d for the case when the output of the first TTL inverter changes from logic 0 to logic 1. The transients can be found in a similar manner for a change from logic 1 to logic 0. This is shown in Figure 5-38e.

5.6.8.2 Lattice Diagram Implementation of the reflection waveform can be achieved with the following tabular approach. This approach is called the lattice diagram. Use Figure 5-39 for reference.

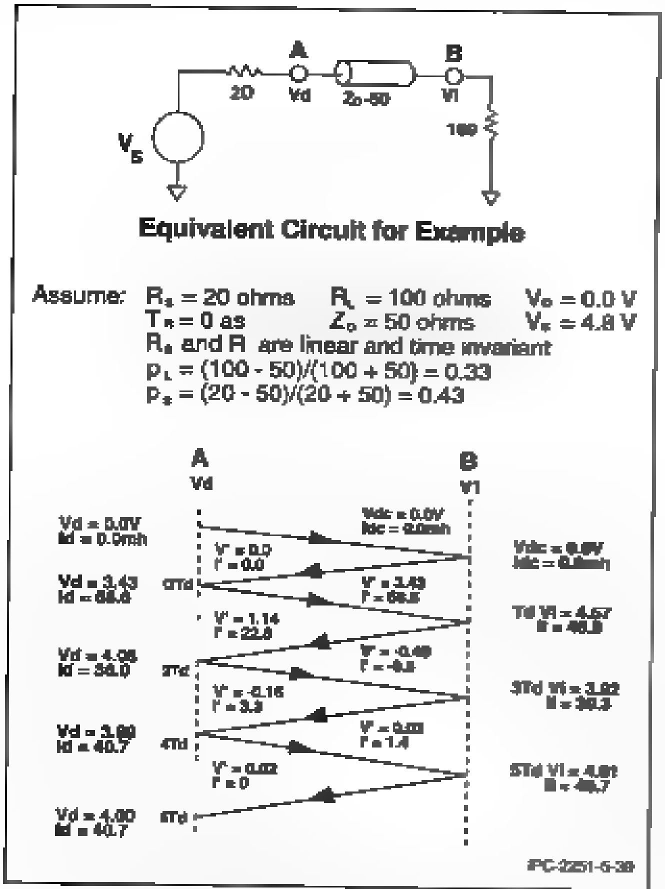

A
B
20
Vd
Zo-50
Vl
100
V_S
Equivalent Circuit for Example
Assume: R_s = 20 ohms R_L = 100 ohms V_o = 0.0 V
T_R = 0 as Z_o = 50 ohms V_s = 4.8 V
R_s and R are linear and time invariant
ρ_L = (100 - 50)/(100 + 50) = 0.33
ρ_s = (20 - 50)/(20 + 50) = 0.43
A
Vd
B
V1
Vd = 0.0V
Id = 0.0mA
Vdc = 0.0V
Idc = 0.0mA
V' = 0.0
I' = 0.0
Vdc = 0.0V
Idc = 0.0mA
Vd = 3.43
Id = 68.6
0Td
V' = 3.43
I' = 68.6
V' = 1.14
I' = 22.8
Td Vl = 4.57
Il = 45.8
Vd = 4.08
Id = 34.0
2Td
V' = -0.49
I' = -9.8
V' = -0.16
I' = 3.3
3Td Vl = 3.92
Il = 39.3
Vd = 3.99
Id = 40.7
4Td
V' = 0.05
I' = 1.4
V' = 0.02
I' = 0
5Td Vl = 4.01
Il = 40.7
Vd = 4.00
Id = 40.7
6Td
IPC-2251-5-39

Figure 5-39 Equivalent Circuit Example (top) with Corresponding Lattice Diagram (bottom)

The lattice diagram is initiated by drawing the signal line under evaluation with the source on the left and the load on the right. The output of the source is labeled "A" and the input of the load "B." Vertical lines are then drawn below points "A" and "B." These lines indicate the difference in length, "D," and propagation time $t_d = t_{pd}D$.

The first calculation step is to determine the reflection coefficients ρ_s and ρ_L.

Next determine the initial condition of the line. This will be the steady state voltage V_{DC}.

where:

$$V_{DC} = V_S(0\text{-})\frac{R_L}{(R_L + R_S)} \qquad [0.87]$$

At time T+0, V_S has transitioned (since t_r = 0 ns) and the voltage at point A will be determined by equation [0.56] V_B will still be equal to V_{dc}. At T = T_D, V_B is

$$V_B = V + V_{DC} \qquad [0.88]$$

$$V_B = \rho s V_L + V_{DC} \qquad [0.89]$$

Each reflection for T = 2td to Ntd will follow the same pattern as above. The process continues until the steady state voltage is obtained.

Characteristics of the Lattice Diagram are:

- Linear, time invariant resistance must be used
- Method is long and tedious to perform by hand
- Easily converted into a computer program
- The resultant waveforms at the load and driver end of the signal line are shown in Figure 5-40.

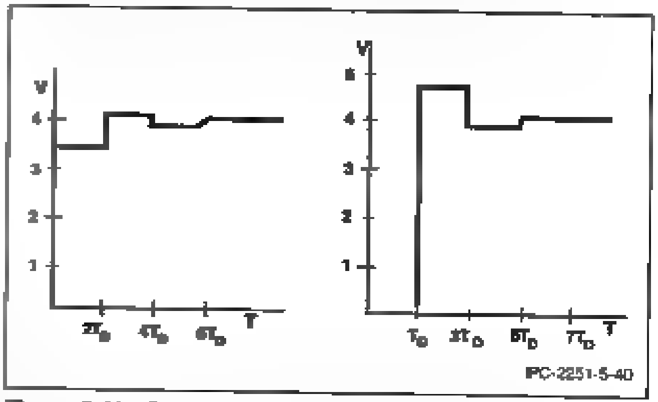


Figure 5-40 Predicted Driver (A) and Load (B) Waveforms for Figure 5-39

5.7 Crosstalk Due to the dense packaging and fast edge transitions of the selected logic families, noise due to crosstalk must be included in the signal AC noise budget. This section presents an in-depth model and equations for determining the magnitude of crosstalk.

5.7.1 Model The coupling of adjacent signals from active lines to a passive line creates crosstalk noise. These lines are in close enough proximity as to create as appreciable mutual capacitance (C_M) and mutual inductance

(L_M). The model of two lines in a crosstalk environment is illustrated in Figure 5-41. To cancel the effect of reflections in the model both lines are terminated to their characteristic impedance, Z_O. Both lines also have equal inherent propagation delays of T_D.

The following discussion references Figure 5-41. A pulse of magnitude V and edge transition rate "a," (typically V/ns) is transmitted down the active line from point S. When it arrives at point X_1 currents are produced on the passive line due to mutual capacitance and inductance.

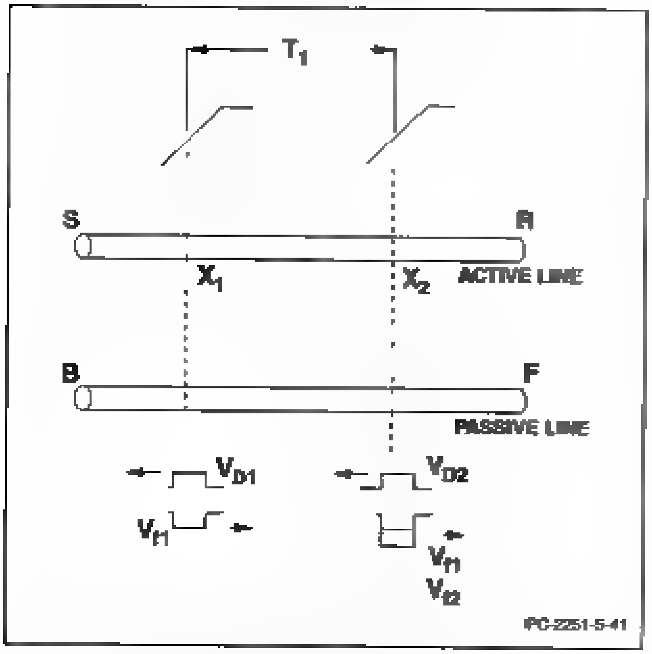


Figure 5-41 Induced Crosstalk Voltages

Since the mutual capacitance sees equal capacitance either way on the passive line, equal and opposite currents, I_C, are produced. Simultaneously, according to Lenz's Law, an equal but opposite inductive current, I_L, will be induced on the passive line.

At point B the currents, I_C and I_L, are additive and will produce a voltage of the same polarity as the active line. At point F the currents are opposite. Since the line is in a nonhomogenous environment I_C and I_L will not cancel each other. In general, I_L is greater than I_C. The summation of currents will, therefore, create a voltage of an opposite polarity than the active line at point F.

Assuming that $2t_d$ > "a," the pulse on the active line will take t_d to propagate to point R at the end of the line. (Line length referred to here is the length of adjacency.)

Consider the point in time that the pulse reaches X_1 of Figure 5-41. As was shown previously, two rectangular pulses that are proportional to the derivative of the active pulse will be created on the passive line. One pulse, V_{BL}, is a result of I_C plus I_L. It will propagate back towards point B This will be the same polarity as the pulse on the active line.

A second pulse, VFL, is a result of I_C minus I_L. It will be created and will propagate towards point F This pulse will be opposite in polarity than the active pulse. After time T_1 the active pulse arrives at X_2. As before, the two pulses are created. During this time V_{F1} has propagated the same distance as the active pulse and will add onto V_{F_2}. As the active pulse travels down the rest of the active line all n of the V_{FN} pulses will add until the active pulse reaches the end of the line. This pulse is defined as forward crosstalk. As can be seen, its magnitude is proportional to the amount of coupling at each point X_N (the coupling ratio is the forward crosstalk constant, K_F) and the length of the line. The width of the pulse will be equal to the risetime of the active pulse. The pulse that is the result of the addition of I_L and I_C that was created at point X_1 travels toward point B. When the active pulse arrives at X_2, T_1 time later, another identical pulse is created and also starts traveling towards point B. The pulse at X_1 will then be $2T_1$ ahead of V_B. As the active pulse travels down its line a succession of pulses $2T_1$ apart will be induced on the passive line propagating towards point B. Therefore, point B will see a series of pulses for a time $2T_D$ after the risetime "a" of the active pulse. The magnitude of the pulse will be independent of the line length but will be proportional to the amount of coupling which creates the backward crosstalk (the coupling ratio is the backward crosstalk constant, K_B).

If a >$2T_1$, the backward crosstalk will be attenuated by $2T_1$/a. The forward crosstalk pulse will also be attenuated by 1/a. Figure 5-42 shows the expected forward and backward crosstalk pulses for a properly terminated line.

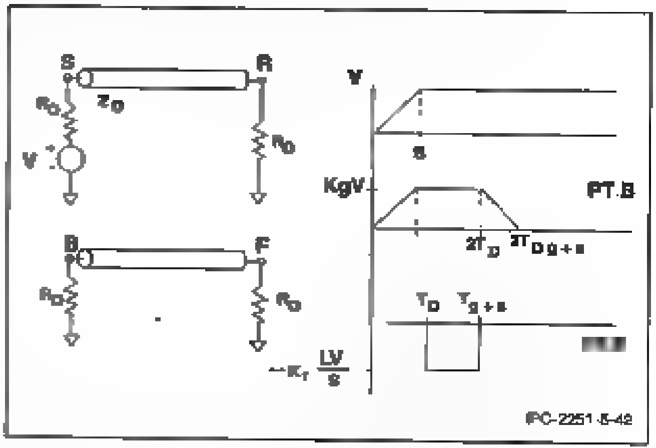


Figure 5-42 Crosstalk Voltages for a Line Terminated at Both Ends

For a line length greater $2t_d$ the forward and backward cross-talk coefficients, K_F and K_B are

$$K_F \quad V_F\left(\frac{a}{VD}\right) \qquad [0.90]$$

$$K_B = \frac{V_B}{V_I} \qquad [0.91]$$

where:

V_F = Forward crosstalk voltage
V_I = Voltage switch on active line
a = Edge transition time
D = Length of coupled region
V_B = Backward crosstalk voltage

5.7.2 Microstrip Transmission Line The forward and backward crosstalk coefficients are related to the impedance of the signal lines and the mutual inductance and capacitance between them. Values for both can be derived from the following equations.

$$K_B = C_0Z_0\frac{(K_L + K_C)}{4t_d} \qquad [0.92]$$

$$K_F = -0.5C_0Z_0\,(K_L - K_C) \qquad [0.93]$$

$$K_L = 0.55e\left[-\left(A2\frac{s}{h}+B2\frac{w}{h}\right)\right] \qquad [0.94]$$

$$K_C = 0.55e\left[\left(A1\frac{s}{h}+B1\frac{w}{h}\right)\right] \qquad [0.95]$$

where:

$$A1 = 1 + 0.25\ln\left[\frac{(\varepsilon_r + 1)}{2}\right] \qquad [0.96]$$

$$A2 = 1 + 0.25\ln\left[\frac{(\mu_r + 1)}{2}\right]$$

$$B1 = 0.1\sqrt{(\varepsilon_r + 1)}$$

$$B2 = 0.1\sqrt{(\mu_r + 1)}$$

S -- Line spacing

To generate the maximum crosstalk values for the victim line some knowledge of the load configurations must be known. To determine the effect of the induced crosstalk pulses on the loads the AC noise immunity characteristics of the loads and the crosstalk noise budget allocation must be known.

5.7.3 Embedded Microstrip Transmission Line The crosstalk equations for an embedded microstrip are the same as for the microstrip with the difference of a modified $\varepsilon_{r,eff}$. For a line length greater than 2 x T_D the forward and backward crosstalk is the same as equations [0.90] and [0.92] with A1 equal to equation [0.97].

$$A1 = 1 + 0.25\ln\left[\frac{(\varepsilon_r' + 1)}{2}\right] \qquad [0.97]$$

$$\varepsilon_r' = \varepsilon_r\left[1\text{-}e^{-1.55\frac{h'}{h}}\right] \text{ from equation [0.25]} \qquad [0.98]$$

where:

h' = Distance from reference plane to the top of the dielectric
h = Distance from reference plane to the signal line

5.7.4 Backward Crosstalk Amplitudes

$$V_{bx} = \left(\frac{k+1}{2}\right)\left(\frac{Z_0}{2Z_m}\right) \text{ for } t \le 2\tau \qquad [0.99]$$

$$V_{bx} = \left(\frac{k+1}{2}\right)\left(\frac{Z_0}{2Z_m}\right)\left(\frac{2\tau}{t}\right) \text{ for } t \le 2\tau \qquad [0.100]$$

$$V_{fx} = \left(\frac{k-1}{2}\right)\left(\frac{Z_0}{2Z_m}\right)\left(\frac{2\tau}{t}\right) \qquad [0.101]$$

$$Z_m = \frac{120}{\sqrt{\varepsilon_r}}\left(\frac{f_1\,(f_2)}{f_1 \quad f_2}\right) \qquad [0.102]$$

$$f_1 \quad \ln\left(\frac{4h}{d}\sqrt{1+g^2}\right) \qquad [0.103]$$

$$f_2 = \ln\left[\left(\frac{4h}{g\,(d)}\right)\left(\frac{1}{\sqrt{1+\frac{1}{g^2}}}\right)\right] \qquad [0.104]$$

$$g = \frac{2h}{S} \qquad [0.105]$$

Variables

Z_0 = Characteristic impedance (in ohms)
Z_m = Mutual impedance between lines (in ohms)
s = Wire spacing center to center (in mils)
$\varepsilon_{r,eff}$ = Effective dielectric constant
d = Wire diameter (in mils)
h = Wire height - center to plane (in mils)
k = Constant to adjust for dielectric geometry (F 1.025)
t = Signal rise time (in nanoseconds)
V_{bx} = Backward crosstalk (Volts/V)
V_{fx} = Forward crosstalk (Volts/V)
τ = Parallel coupled region (in ns)
L = Parallel coupled length (in inches)

5.7.5 Stripline In the stripline environment the forward crosstalk equals zero. This is due to K_L being equal to K_C. The back crosstalk will be twice the equivalent microstrip crosstalk (where the impedances are the same) because the capacitance is twice as high.

$$K_B = 2\left(\frac{V_B}{V_I}\right) \qquad [0.106]$$

or,

K_B is given in [0.91]

$K_F = 0$

Since the line is centered between the reference planes h is the distance from the signal line to either plane.

The crosstalk environment for the asymmetric line is the same as the stripline. Crosstalk between signal layers is negligible because the layers are orthogonal to each other.

5.7.6 TTL/MOS Models There are two configurations in which two lines with one driver and one receiver will have a common run. The first is with the drivers at the same end. The second is with the drivers at opposite ends.

Since the "0" state noise level is the most critical all the outputs and inputs common to the passive line used in the following analysis will be at this logic level. Figure 5-43 illustrates the condition with both drivers at the same end. Figure 5-44 illustrates the condition with the drivers at opposite ends.

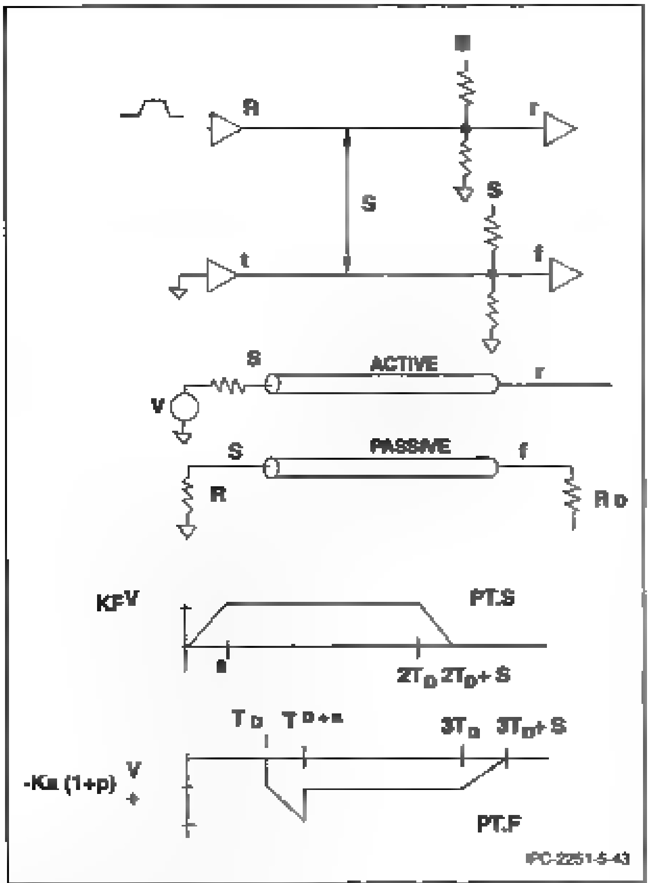


Figure 5-43 Drivers and Receivers at a Common End
a. Physical Implementation
b. Model
c. Backward Crosstalk
d. Forward Crosstalk

When multiple lines are in parallel the noise coupled onto the passive line is additive but time synched. That is, if pulses on adjacent lines are next to the same location on the passive line at the same time, the resulting noise pulses will be directly additive.

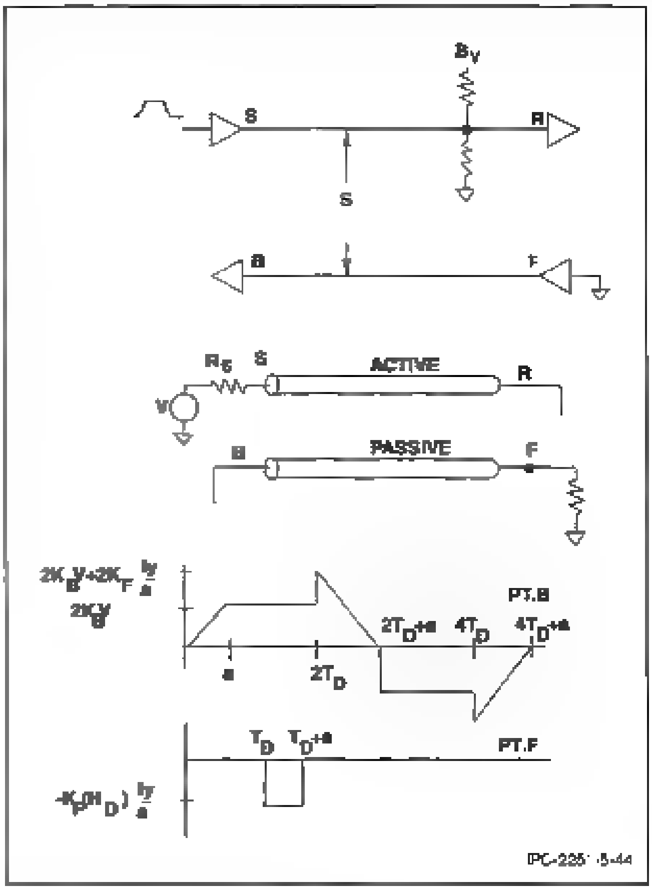


Figure 5-44 Drivers and Receivers at Opposite Ends
a. Physical Implementation
b. Model
c. Backward Crosstalk
d. Forward Crosstalk

The crosstalk pulse may have relatively high amplitude and not cause any circuit problems. This is due to the inherent AC noise immunity of TTL devices. Figure 5-45 presents the AC noise immunity curves for some TTL logic families. These curves coupled with the fact that the noise pulse due to crosstalk will usually be narrower than the gate propagation delay will allow a large pulse at the input to the device, without affecting the contents or the output.

5.8 Signal Attenuation The two principal causes of signal attenuation are resistive losses due to the conductor, and dielectric losses. These two loss mechanisms will be discussed separately in the following two sections.

5.8.1 Resistive Losses (Skin Effect) For a conductor carrying an alternating electric current, the distribution of the current over the cross section of the conductor is nonuniform. The current density is greater at the surface of the conductor than at its center. This phenomenon, which is

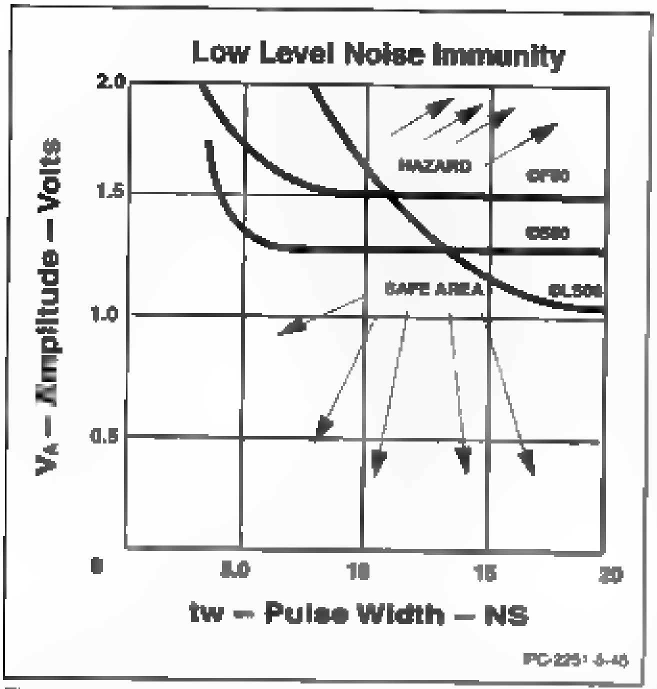


Figure 5-45 AC Noise Immunity for Selected TTL [illegible]

known as the skin effect, is due to electromagnetic (inductive) effects and becomes more pronounced as the frequency of the current is increased. The distance, δ, at which the current density decays to 1/e of its value at the surface is called the skin depth, and is given by [0.107]:

$$\delta = \frac{1}{\sqrt{\pi f \sigma \mu}} \qquad [0.107]$$

where:

f is the frequency in Hz
σ is the conductivity in mhos/m
μ is the absolute permeability of the conductor in H/m

Thus, the effective resistance of a conductor carrying an alternating current is greater than the direct current resistance and, consequently, the power losses are greater than the usual I^2R, and rise proportionately with the square root of frequency. The effective surface resistivity, R_s, of a conductor is given by:

$$R_s\,(\text{ohms}) = \frac{1}{\sigma\delta} \qquad [0.108]$$

which on substitution for δ gives:

$$R_s = \sqrt{\frac{\pi f \mu}{\sigma}} \qquad [0.109]$$

For copper, assuming a conductivity of $\sigma = 5.8 \times 10^7$ mhos/m and its permeability to be that of free space ($4\pi \times 10^{-7}$ H/m), this leads to:

$$R_s = (2.61 \times 10^{-7})\sqrt{f} \qquad [0.110]$$

The resistance, R, of a conductor of length, D, and circumference, C, is given by:

$$R\,(\text{ohms}) = \frac{D\,(R_s)}{C} \qquad [0.111]$$

This resistance may be used, with the usual I^2R relationship, to calculate the resistive power loss.

However, two cautionary notes must be added.

As a consequence of the micro roughness of the metal, the effective length of the conductor may be longer than its physical length, and the extent of the resistive power loss can be expected to vary with different conductor surface finishes. In addition, an assumption implicit in the above, is that the field lines extend uniformly from the conductor in all directions. This assumption is only completely accurate for a conductor of circular cross section, surrounded by a ground potential at infinity. For realistic circuit configurations, concentrations of field lines will be greater in some regions than in others, and this will lead to second order effects. For a more complete discussion of resistive losses for the stripline configuration the reader is referred to Howe (1974).

5.8.2 Dielectric Losses Energy is also absorbed by the dielectric medium surrounding the conductors. For the stripline configuration, signal attenuation by the dielectric is given approximately by:

$$A_D = \frac{27.3\,(\tan\delta)\,\sqrt{\varepsilon_{r,eff}}}{\lambda_0} \qquad [0.112]$$

where:

λ_0 = free space wave length
$\varepsilon_{r,eff}$ = effective relative permittivity and
tan δ = loss tangent

Consequently, in order to minimize signal attenuation by the dielectric, it is desirable to select materials and the electrical configuration such that both $\varepsilon_{r,eff}$ and tan δ are as low as possible. For other circuit configurations the above expression must be modified to replace tan δ with an effective tan δ_{eff}.

5.8.3 Rise Time Degradation Both of the principal mechanisms by which energy is absorbed from a propagating signal become more severe with increasing frequency; resistive losses are proportional to the square root of frequency, while the amount of energy absorbed by the dielectric medium is directly proportional to f. Consequently, the higher the frequency of propagating signals the more closely losses and noise budgets should be examined.

In addition, for digital circuitry, this frequency dependence has ramifications upon the form in which pulse-shape corruption is manifested. A digital pulse may be represented by a sum of its Fourier components. Clearly, the higher frequency components of a transmitted pulse will be attenuated most rapidly. The highest frequency of concern, or bandwidth (BW) in Gigahertz, of a pulse of finite rise time, is given by:

$$\text{BW (GHz)} = \frac{0.35}{t_r} \qquad [0.113]$$

where, t_r in nanoseconds is the pulse rise time from 10% to 90% of its maximum value. Consequently, as the higher frequency components are absorbed, the bandwidth of the propagating pulse will decrease, producing a degradation of the rise time. Such rise time degradation is usually the most important effect of signal attenuation in digital circuits.

5.9 Computer Simulation Program The equations and techniques described in Section 5 can be complex and difficult to solve manually. A list of commercially available computer simulation programs that may be used for high-speed designs is available online through www.ipc.org. Other programs are available and will be included as the IPC is notified. (This list is not comprehensive, nor endorsed by the IPC.)

5.9.1 Computer Simulation Models For most computer simulation programs, a device model is required for proper operation and results. Generally, a SPICE model or IBIS model is used to provide the required data to the simulation program. There are many SPICE programs and models for devices on the market. Recently, IBIS models are being used due to their nonproprietary nature and availability. A model is required for each device in the design and sometimes for the transmission line if the tool does not calculate its parameters.

5.9.1.1 SPICE Model A model used for circuit analysis with the Berkeley SPICE simulation engine and others. Primarily used for analog or detailed simulations of small-scale digital circuits or systems. Models range from simple ideal circuits to extremely complex systems. The models are made up from all the fundamental elements of electronics e.g., resistors, capacitors, inductors, also voltage, current, transconductance sources, etc; providing the framework to construct hierarchical simulations of models and sub circuits. SPICE models are generally available from the device manufactures.

5.9.1.2 IBIS Model A model used for Signal Integrity analysis that defines a device package inductive, capacitive, and resistive elements; input and output capacitance; power and ground clamp voltage and currents; input voltage levels and measurement threshold; output voltage, current levels, and output ramp voltages; and edge rates (dV/dT). IBIS models are available from the device manufacturer or from many Internet Websites. Some IBIS models are converted from SPICE models. Converted SPICE to IBIS models may contain errors such as nonmonotonic edges that should be corrected before use. If an IBIS model has to be created from scratch, an IBIS Golden Parser or similar application program should be used to insure the IBIS file has the proper elements for use. The specification for IBIS is an evolving specification for industry needs and is controlled by the IBIS committee.

5.10 Connectors

5.10.1 Sensitivity Connectors located within a conductive path are transparent to signals, a lumped element, provided that the signal bandwidth is not equivalent to, or less than the physical mated length of the connector. In digital switching systems, the rise time of the pulse, a gating factor, is used to determine the cutoff frequency ($f_0 = 0.35/t_r$). Signal bandwidth is derived from the equation $\lambda = v/f_0$. The connector is lumped if the connector path length is < $\lambda/15$ and distributed if the connector path is not. A distributed element must have transmission criteria applied to eliminate signal distortion.

5.10.2 Distributed Line Compensations Connectors found to be distributed, as described in 5.10.1, should compensate the transmissibility of their medium for all or part of the following issues.

a. Impedance

b. Skew

c. Propagation delay (time)

d. Parasitic elements

e. Grounding

f. Crosstalk

The use of signal modeling software is suggested in order to ascertain the severity of impact on the overall circuit and the necessary compensating corrections.

5.10.3 Connector Types Connectors generally fall into the following electrical usage categories. The cutoff frequencies and bandwidths shown in Table 5-6 are generalizations of the category. Specific supplier parts will have their own unique values and tolerances owing to design and constructions (e.g., path length).

5.11 EMI Layout Considerations

5.11.1 Reasons for Considering EMI Layout The requirements for an EMI layout are generally directed by Regulatory Agency requirements for a product to meet required Radiated and Conducted Emissions, and /or Radiated and Conducted Susceptibility limits before the product

Table 5-6 Connector Equivalent Bandwidth

Connector Type	Wavelength (in air)	Cutoff Frequency
Isolated Pin	3 km	100 KHz
Edge card (>0.1 in grid)	30 m	10 MHz
Open pin (0.1 in & signal/ ground arrangement)	3 m	100 MHz
Reference plane	200 mm	1.5 GHz
Coax	3 mm	100 GHz
Waveguide	30 µm	10 THz
Fiber Optics	0.7 µm	400 THz

may be marketed or sold in that country. Some of those Regulatory Agency requirements are FCC Class A/B, EN 55022 Class A/B, (CE Mark), VCCI Class 1/2, MIL-STD-461E, RTCA DO-160, UK Defense 58-6/1, etc. Other reasons dictate an EMI layout such as self-operation with adjacent cards in a card rack, electrically noisy environments, etc. Care must be exercised that EMI layouts do not conflict with Safety Regulatory Agency requirements (high ground leakage currents from capacitors). Since the active components on a Printed Wiring Board (PWB) generate EMI, they can generally be controlled to acceptable levels through source suppression practices in the layout. System level EMI layout (casework for EMI containment, interface cable partitioning, etc.) is beyond the scope of this document.

Many of the EMI layout practices below are inter-linked and should be considered.

5.11.2 Digital Edge Rates To provide products with higher speed performance, Clock and Data Rates will increase. To provide faster Clock and Data rates, edge rates need to be faster to accommodate the required logic Set-up and Hold timing for proper logic operation. As stated in 5.2.3, the highest frequency component of a digital pulse is the transition edge (Rise Time or Fall Time). With some output structures, the Rise and Fall Time are equal. Generally, one edge is faster than the other, both edges are modified by trace length, loading, and driver technology.

As Rise and Fall Times on active devices become faster (decrease), the requirement for attention to EMI layout practices increase. EMI layout practices may include controlling component placement, signal line termination, signal line routing, plane partitioning, crosstalk management, power decoupling, and shielding. When considering EMI layout, edge rates are the primary concern. With an EMI design, it is almost always desired to have the slowest edge rate possible thereby limiting the high frequency spectrum. Integrated Circuit manufacturers typically desire more devices per manufacturing wafer to increase yield and reduce production costs. The more devices per wafer reduces the individual device feature size (transistor/FET and interconnect sizes), which in turn increases the device's internal and external edge rate speeds. This complicates the EMI design of a product as even slow clock and data rates will have fast edges that need to be source suppressed in the design. The low voltage technologies (like LVDS) help by lowering the voltage swing and thus emitted levels.

5.11.3 Suggested EMI Layout Practices The following sections suggest ways in which EMI layouts may be included in a product.

5.11.3.1 Controlling Component Placement Controlling the component physical placement is necessary to partition high rate edge generators (fast devices like clock drivers) away from the board edge. A good practice is to place like logic families together as a functional group. Place cable interface drivers near their associated I/O connector. Avoid mixing logic families in the same plane partition (TTL with ECL or TTL with GTL). Plan ahead for short routes, a rough placement diagram may indicate where small schematic changes (gate or pin swapping) will dramatically improve the layout. Clock Oscillators and Clock distribution (Clock Trees) should be placed close to preserve edge rate and confine EMI energy.

5.11.3.2 Signal Line Termination A properly terminated signal line emits less EMI and is less susceptible to EMI fields. Care should be exercised that all high rate edges (almost all signal lines in current products) are properly terminated into their respective impedance. A line that is not terminated will generate a reflection, which if not controlled radiates, couples to adjacent traces, contaminates plane partitions, and couples to interface or power cables which exit the product enclosure and cause EMI test or susceptibility failures.

It is best to insure the I/O Interface cabling impedance matches the driver impedance and that the receiver is properly terminated. Cable shields should be properly terminated to contain EMI emissions.

5.11.3.3 Signal Line Routing Proper routing of signal lines is very important. As a trace is routed one must consider that the trace will reference one or two reference planes. Those planes may be power or ground planes. The reference plane(s) are the RETURN CURRENT PATH for the signal line. The plane(s) becomes part of the impedance for the trace and concentration of return current fields need to be well thought out. Large Address or Data Busses generate greater current density in the planes than do random control traces. It should be noted that, when routed voltages are used, they have return current paths as well. Signal lines should not reference different voltage planes or routed voltage traces than the driver, i.e., 5V signal lines should not reference a -2V, -5.2V, -12V, +12V routed voltage trace or plane. Transition noise or power supply noise from the other voltage may cause problems.

Trace routing for clocks and high rate signals should be internal routes between planes (striplines) to provide EMI shielding and to control noise coupling to them. Extra line spacing from these lines to other lines should be used to prevent coupling. Routing clocks on outside layers (microstrip) for long distances should be avoided. General guidelines identified elsewhere in this document should be used to avoid stubs and other Signal Integrity effects which may cause EMI levels to increase.

Routing signal lines across voids in partitions should be avoided if possible, an alternate return current path will result which depending on the trace length, may cause EMI problems. Routing of traces under sensitive circuitry like OP-AMP's, PLLs and Loop Filter components, Synthesizer chips, Video Clock Generators, RF devices, etc., should be avoided.

Avoid routing high rate signal lines near the PWB edge as it may be difficult to provide a return path near the PWB route border. The reference plane(s) for the trace should extend 1.5 to 2 times the trace width beyond the trace to provide an adequate return current reference. This may need to be adjusted to suit higher voltage swings or faster edges.

Power traces to active devices should be as short as possible and as wide as possible (within assembly soldering guidelines) to insure a low inductance (impedance) source for the device.

5.11.3.4 Plane Partitioning It is often necessary to partition the power or ground planes in a design to manage voltage and ground distribution. Copper planes may be partitioned (split into more than one section) to provide TTL and ECL voltages or grounds, etc. Other plane partitions that may be considered are GTL logic partitioning from TTL (to keep the lower level GTL signals in a quiet area), TTL from ECL (for logic family isolation), TTL from analog (to keep TTL edges away from OP-AMP high impedance sensitive circuitry) TTL from video (to keep the video clean), etc.

Unlike plane partitions should not overlap each other, for example, having a TTL ground plane partition on one layer and an ECL voltage plane partition on another adjacent layer. This creates plane coupling that may cause EMI and Signal Integrity problems.

It is best to keep plane inductance as low as possible. Insure the current demands can be met with low voltage drops to all devices. Decoupling will help with instantaneous current demands.

5.11.3.5 Crosstalk Management Crosstalk occurs when traces are placed in close enough proximity that a trace couples edge signals from one trace to the other. The magnitude of crosstalk is based on the fastest edge rate, trace impedances (field coupling to the nearest plane), loading, and the coupled length. Crosstalk problems can be difficult to locate and are best solved by avoiding them in the layout. It is best to identify the signal lines that have higher edge rates (clocks, strobes, etc.) and plan for extra line space for those lines to all other lines. Routing high rate lines on outside layers should be avoided as crosstalk goes up on the outside layer due to only one reference plane for field containment.

Crosstalk can occur from signal lines to I/O Interface lines that exit the enclosure and may cause EMI limit failures or EMI susceptibility problems.

5.11.3.6 Power Decoupling All digital packages should have High Frequency Decoupling Capacitors to insure that edge energy reserves are available for driver transitions. How many high frequency decoupling capacitors is dependent on power and ground pin distribution, drive requirements, predicted noise environment, and board space limitations. Consult the manufacturer or data books for the device. Without High Frequency Decoupling, many of the switching currents will remain on the planes or power /ground traces (if they are long) and cause EMI and functional problems.

High frequency decoupling capacitors should be placed as close to the power and ground pins as possible. High Frequency Decoupling Capacitors on the opposite side of the PWB directly under the Power and Ground pins on the device works best.

Bulk low frequency decoupling capacitors store/source energy for the high frequency decoupling capacitors and provide reduced plane inductance for the PWB. Plan the bulk decoupling to source the high frequency decoupling in an "area of influence" method and place them according to predicted current flow.

Bulk Low Frequency Decoupling and High Frequency decoupling should be provided close to the power input connector for all applicable voltages. This provides clean power for the PWB and reduces any EMI that could couple to power cabling.

Clock Oscillators, Clock Drivers, PLL Power and Grounds, some I/O drivers, on-card Power Inverters, etc., should have a Pi filter power source. This is usually constructed of a High Frequency Decoupling capacitor and Low Frequency Bulk Decoupling capacitor feeding a Ferrite Bead (for isolation), and a High frequency Decoupling capacitor(s) (for edge and quiescent current demands) fed by the other side of the Ferrite Bead, located at the power pin of the device. Be sure the Ferrite Bead will handle the current without saturation. Ferrite bead impedance goes down with increased current (see 5.1.4.5).

5.11.3.7 Shielding Shielding like partitioning improves radiated emissions and susceptibility of the product. By providing local shielding, circuitry is isolated from another offending circuit or from causing a problem with other circuitry. A shield may be a metal fence, via fence, metal cover, guard bands around sensitive traces, chassis ground layers on the outsides of the PCB, etc.

Metal covers typically shield RF circuitry as many of the traces may be surface microstrips and they may radiate or may have noise coupled into them causing problems.

Guard bands are ground traces that surround a trace to provide isolation from other traces on that layer or adjacent layers. The trace is typically wide and grounded by vias periodically to keep the trace at ground potential. If this is used, place the proper distance from the guard band and the trace of interest to preserve edge rate (too close will degrade edge rate or change the impedance of RF traces). A guard band trace if not kept at ground potential at the frequency of interest may magnetically couple to adjacent traces. Sometimes it is best to plan more line space for the signal lines than to use a guard band. Guard Bands are best used for low frequency, low noise applications.

Chassis ground on outside layers if properly grounded to the Chassis provides EMI containment. A good connection to the Chassis is essential and you may want to place a power or ground layer directly below the Chassis Ground layer for signal isolation. This may or may not be a good option with RF boards depending on the grounding arrangements of the system.

6 PERFORMANCE TESTING

With the increase in importance of AC characteristics in the performance of circuit boards, fast and easy tests are needed to verify that the "as built" characteristics are within limits. Two of these characteristics are impedance and capacitance. In order to perform these tests, test structures must be built into test coupons on the outside of each circuit board directly into the circuit boards themselves. The test structures and test methods must be easy to use to insure fast, successful results when performed many times at inspection. This section describes both of these topics and provides some suggested structures and equipment.

6.1 Impedance Testing The impedance of transmission lines in printed boards has an important effect on the high-speed performance of logic systems they contain. Impedance is expressed in ohms and is most often measured using Time Domain Reflectometers (TDRs).

6.1.1 Principle of Impedance Testing Using a TDR The principle on which TDRs operate is to send a very high-speed pulse ($t_r < 200$ ps) down the line being measured. At each change in impedance along the line, some of the energy from the pulse will be reflected back to the source end. A very high-speed sampling oscilloscope is attached at the source to display these reflections. The pulse source has known output impedance, usually 50 ohms, that serves as the reference impedance. The amplitude of each reflection is proportional to the magnitude of the impedance change. The impedance of each segment of the line can be calculated from the percentage of the original pulse that is reflected back to the source.

Section 5 contains a detailed explanation of the reflection phenomenon and the calculations involved in deriving impedance. A more detailed explanation is contained in the operator's manual of each piece of TDR equipment. The operator is advised to read these documents before measuring impedance.

6.1.2 Impedance Measuring Test Equipment Several models of TDR are available from suppliers of high-speed measuring equipment. Some are labeled cable testers, some are labeled simply TDRs, still others are labeled Impedance Test systems and include computers to perform all the calculations required to arrive at the impedance value for a given segment of a line.

6.2 Impedance Test Structures and Test Coupons Impedance measurements can be performed on actual transmission lines in a circuit board or in conductors specially constructed to provide easy access to their ends. Because it is difficult to access the ends of transmission lines in most circuit boards, the specially built lines make impedance testing more convenient and reliable.

6.2.1 Test Structure Design The specially constructed impedance test lines may be designed into the body of the circuit board or into a test coupon designed for this purpose. In either case, the test line must be provided with a terminal at its end to which the test probe is attached. Close by, (2.54 mm [0.1 in] away or with a SMA connector, 3.56 mm [0.14 in] away) an AC ground contact must be provided to insure a good AC return for the test pulses. The length of each test line should be comparable in length to the signal lines with 152 mm [6 in] being a minimum. In order to insure the impedance tests accurately reflect the characteristics of the signal lines, the width and the electrical environment of the test line(s) must be the same as the signal lines and there must be a test line in each signal layer.

It is only necessary to provide contact to one end of a test line in order to make an impedance measurement. However, if contacts are provided at each end a wider assortment of testers and test methods can be employed. Since the area cost of an additional contact point and its associated ground contact is minimal, it is advisable to provide test contacts at both ends of each test line.

6.2.2 Test Probes and Connections Some impedance tests call for connecting subminiature connectors to the line ends. This is not economical in most digital logic boards nor is it necessary. It is possible to connect test probes to the end of the TDR cables that consist of two contacts 2.54 mm [0.1 in] apart or with a SMA connector, 3.56 mm [0.14 in] apart. This type of contact is economical and provides rapid contact to the test structures. Because it is a small structure, it does not introduce discontinuities that materially affect the impedance tests.

6.2.3 Locating Impedance Test Structures As high performance logic circuit boards grow larger and more complex, the complexity of the impedance test structures grow with them. As a result, building these structures into a test coupon becomes less practical. In addition, real estate may not be available in the fabricator's economical panel size in which to build a test coupon. If this occurs, the test coupon may substantially increase the cost of the finished circuit board.

6.2.3.1 Building Test Conductors Into the Printed Board Designing test conductors into a circuit board involves routing conductors on signal layers in areas not being used by the actual logic connections. In almost all cases, this can be done without penalty. In this way, horizontal test conductors will be built into horizontal layers and vertical test conductors into vertical layers.

An advantage of building the test conductors into the body of the circuit board is that the test structures are carried along with the circuit board eliminating the need to provide tracking of test coupons.

6.2.3.2 Designing an Impedance Test Coupon Designing an impedance test coupon involves creating a long, narrow circuit board that is attached to the circuit board to be evaluated along one edge. The attachment point must be small to facilitate easy removal. The test coupon mustcontain all of the signal and power layers contained in the circuit board. The board should be conditioned with respect to the typical operating temperature of the circuit board being designed. Test lines must be built into each layer as described above. Some provision should be made to ensure traceability between the coupon and the circuit boards.

6.2.4 A Simple Impedance Test Method The impedance of a transmission line can be determined by terminating its far end in a terminating resistor of a value that absorbs all of the incident signal, producing no reflection (see Figure 6-2). A straightforward way to do this is to attach the TDR as is done for any impedance test, setting it up so that the reflection from the open line end is at mid-screen. Attach a miniature single-turn noninductive trimpot to the far end of the line between the end and ground. Slowly adjust the trimpot until the line on the display is flat between the line and beyond (no reflection). This is the condition of ideal/perfect termination. Measuring the resistance value of the trimpot with a digital multi-meter (DMM) establishes the impedance of the line under test.

This method is offered because it is quick, accurate and can be done repeatedly without requiring accurate calibration of the equipment and without requiring complex calculations or a computer.

6.3 Stripline Impedance Test Coupon The test coupon below (Figure 6-1) provides a stripline transmission line coupon for each signal layer of the circuit board. The coupon provides a mounting pattern for a standard SMA/SMC board connector with a 0.89 mm [0.035 in] center pinhole. A TDR can be connected to either end for the impedance [redacted]

The test trace can be on an attached coupon or be a trace on the circuit board.

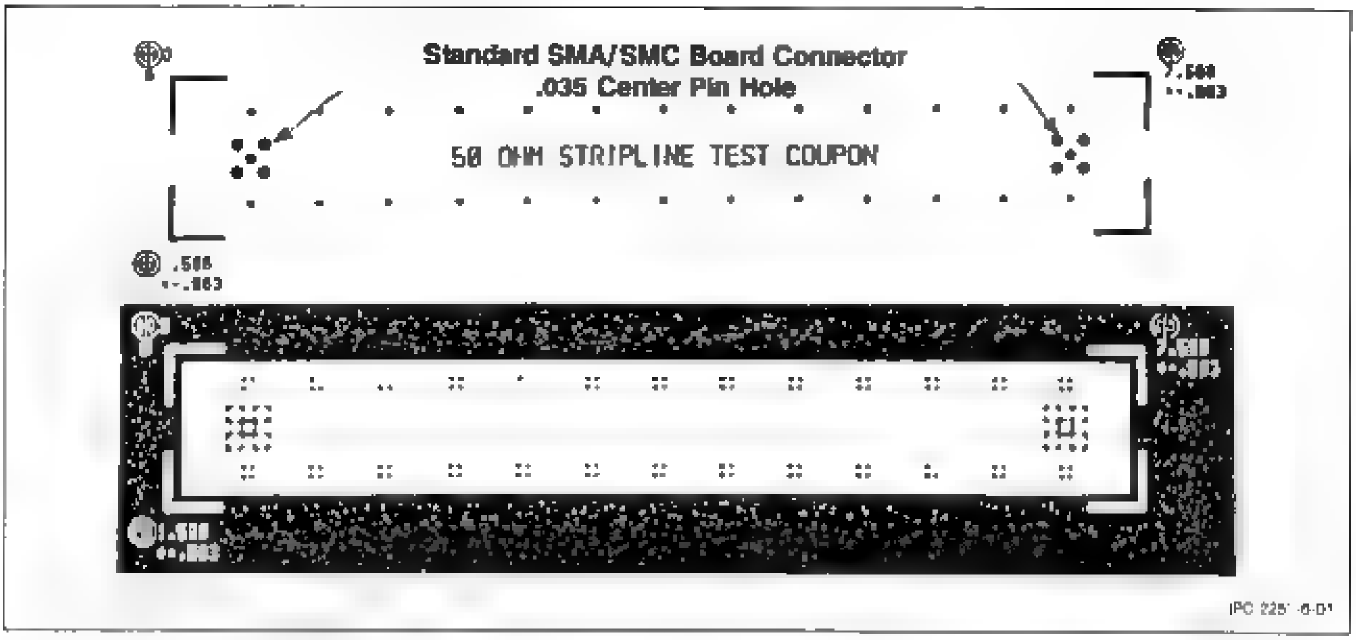
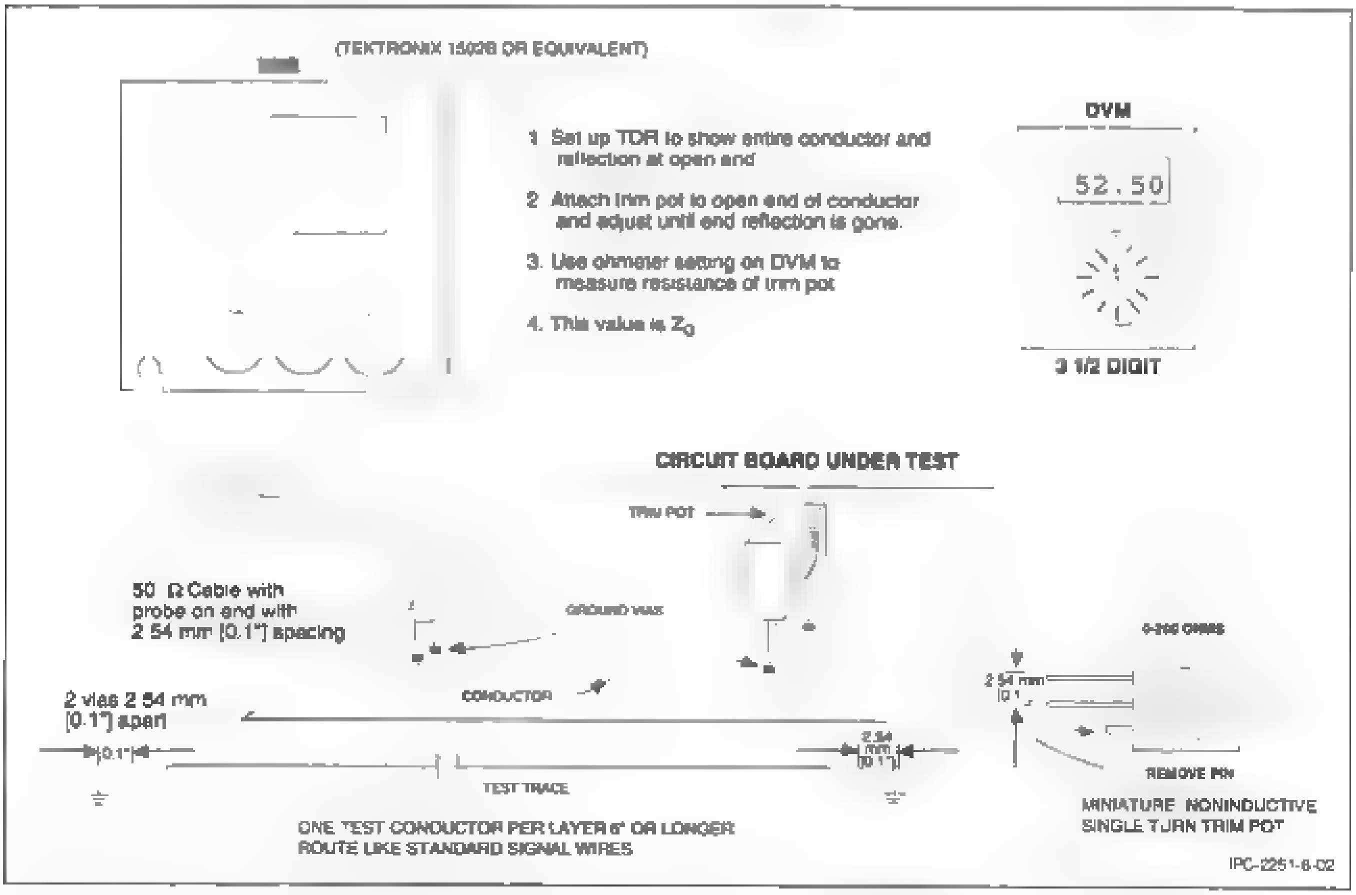

Standard SMA/SMC Board Connector
.035 Center Pin Hole
50 OHM STRIPLINE TEST COUPON
.500
+-.003
IPC-2251-6-01

Figure 6-1 TDR Impedance Test Coupon


(TEKTRONIX 1502B OR EQUIVALENT)
DVM
52.50
3 1/2 DIGIT
CIRCUIT BOARD UNDER TEST
TRIM POT
50 Ω Cable with probe on end with 2 54 mm [0.1"] spacing
GROUND VIAS
0-200 OHMS
2 vias 2 54 mm [0.1"] apart
CONDUCTOR
2 54 mm [0.1"]
[0.1"]
2 54 mm [0.1"]
TEST TRACE
REMOVE PIN
ONE TEST CONDUCTOR PER LAYER 6" OR LONGER
ROUTE LIKE STANDARD SIGNAL WIRES
MINIATURE NONINDUCTIVE
SINGLE TURN TRIM POT
IPC-2251-6-02

1. Set up TDR to show entire conductor and reflection at open end
2. Attach trim pot to open end of conductor and adjust until end reflection is gone.
3. Use ohmeter setting on DVM to measure resistance of trim pot
4. This value is Z_0

Figure 6-2 Test Setup for Measuring Conductor Impedance (Suitable for Receiving Inspection)

Appendix A

DEVICE CHARACTERISTICS

This appendix presents summary tables and graphs that can be used in established digital device high speed performance characteristics. These data are typical and should be used as such.

A.1 74Fxxx Fairchild Advanced Schottky TTL (FAST) is faster, dissipates less power, has a higher more tightly controlled threshold voltage, lower input current, higher output current, and lower input and output capacitance than Schottky TTL. These are bipolar devices packaged in DIP and SM packages.

A.1.1 74Fxxx DC Characteristics

Table A1 74Fxxx Family Characteristics

	Parameter	Value	Units
VIM	MIN Input HIGH Voltage	2.0	Volts
VIL	MAX Input LOW Voltage	0.8	Volts
VOH	MIN Output HIGH Voltage	2.7	Volts
VOL	MAX Output LOW Voltage	0.5	Volts
IOH	MAX Output HIGH Current	-1.0	mA
IOL	MAX Output LOW Current	20	mA
IIH	MAX Input HIGH Current	20	µA
IIL	MAX Input LOW Current	-0.6	mA
IOZH	MAX 3S HIGH OFF Current	50	µA
IOZL	MAX 3S LOW OFF Current	-50	µA
IOS	MAX Output Short Current	-150	mA
XyHL	HL Capacitive Drive	0.03	ns/pf
XyLH	LH Capacitive Drive	0.03	ns/pf
ICCL	Supply Current, LOW	2.35	mA
ICCH	Supply Current, HIGH	0.70	mA
TpLH	LH Propagation Time	3.9	ns (@ 15 pf)
TpHL	HL Propagation Time	3.6	ns (@ 15 pf)
NMH	Noise Margin HIGH	700	mV
NML	Noise Margin LOW	300	mV
FOH	Fanout HIGH	50	
FOL	Fanout LOW	33	
Tr	10– 90% Rise Time (Typ)	1.2	nS
Tf	90– 10% Fall Time (Typ)	1.2	nS
Zom	Line Impedance MIN	35	ohms
CI	Max Input Capacitance	4.0	pf

The typical data presented above is for Vcc = 5.0V ±5% and Ta = 0 to 70°C.

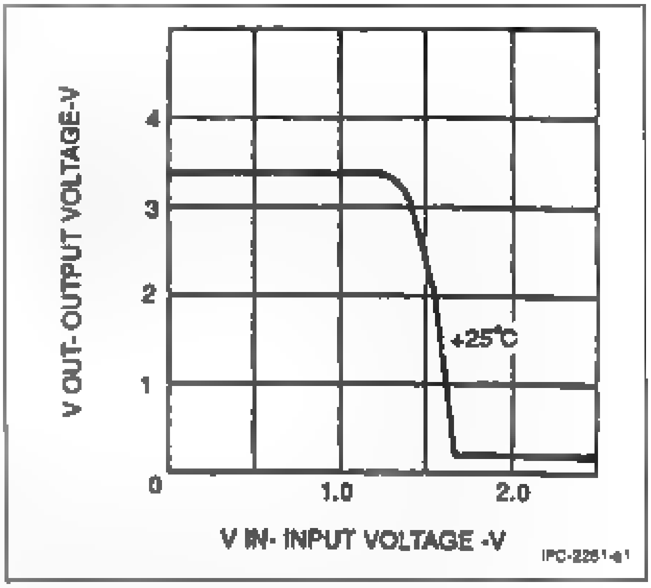


Figure A1 74Fxxx V_O vs. V_I

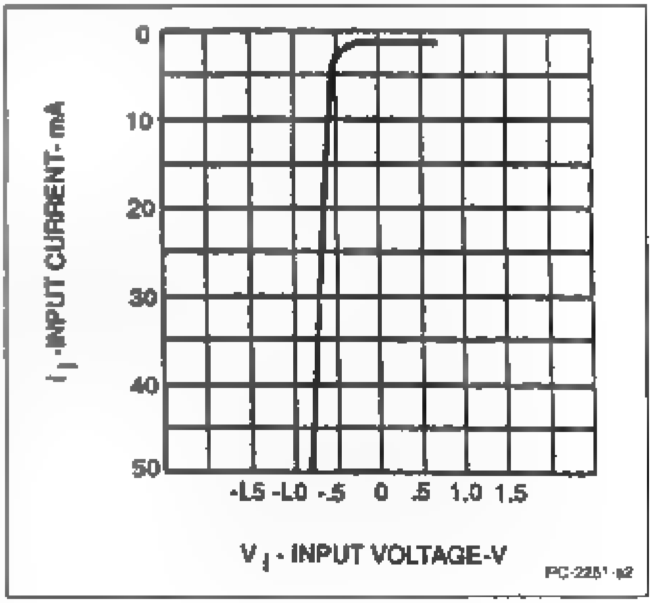


Figure A2 74Fxxx I_O vs. I_I

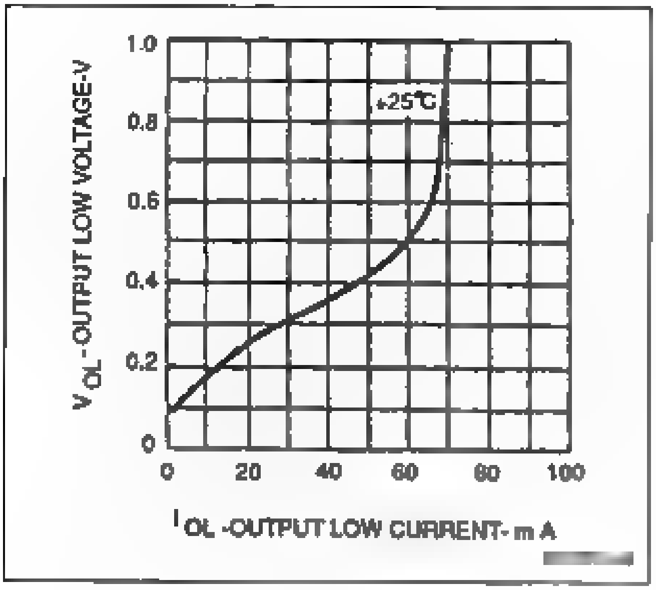


Figure A3 74Fxxx V_{ol} vs. I_{ol}

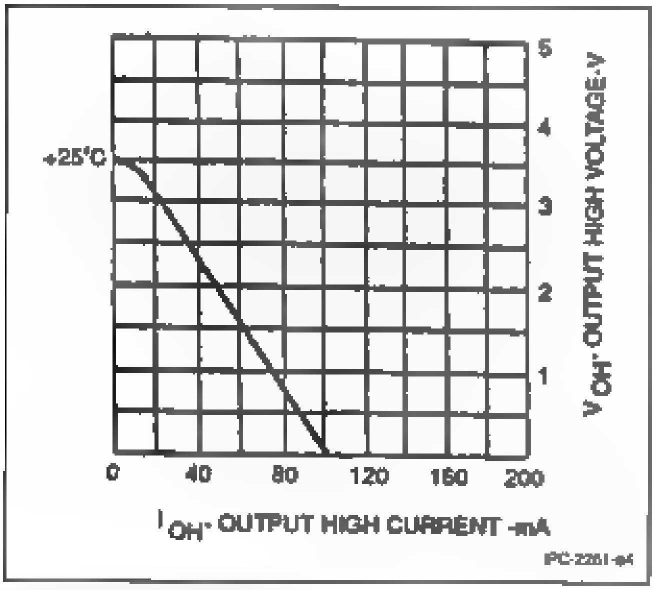


Figure A4 74Fxxx V_{oh} vs. I_{oh}

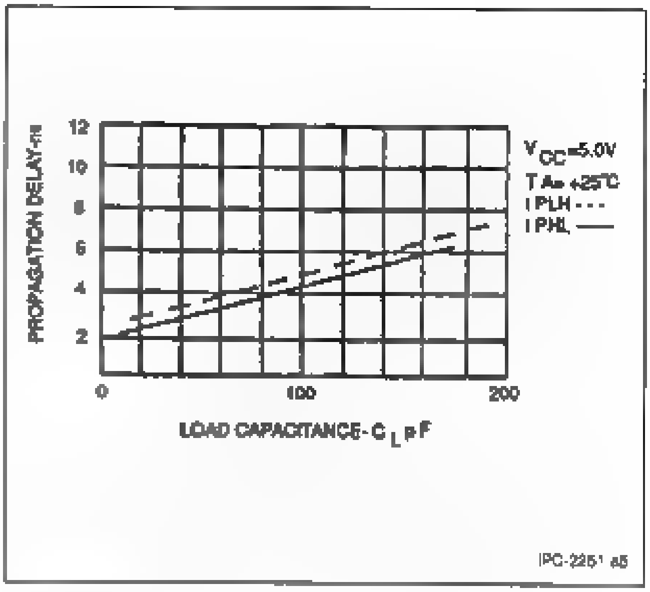


Figure A5 74Fxxx Propagation Delay vs. Load Capacitance

A.1.2 74Fxxx AC Characteristics

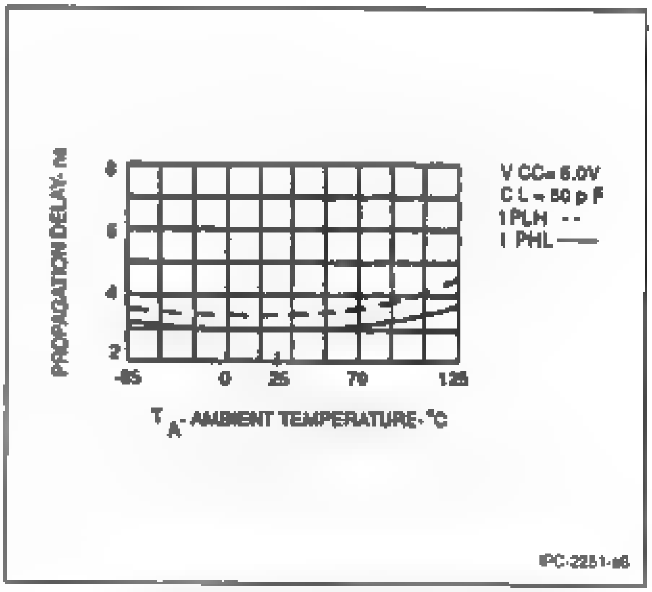


Figure A6 74Fxxx Propagation Delay vs. Temperature

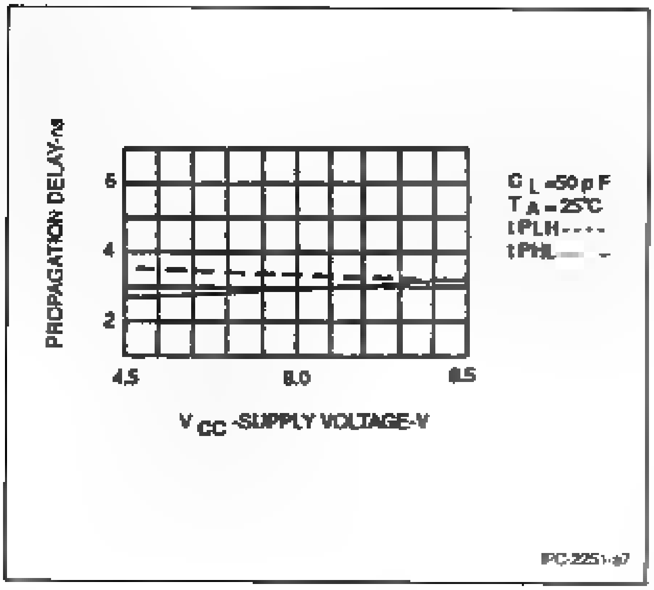


Figure A7 74Fxxx Propagation Delay vs. Vcc

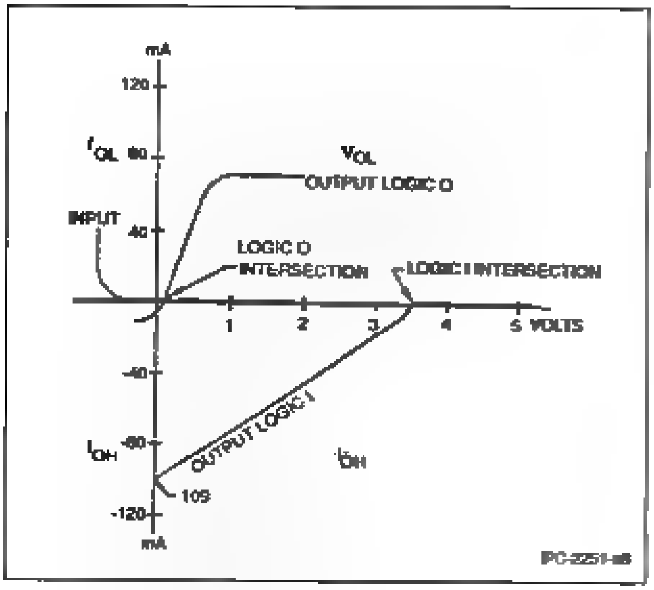


Figure A8 74Fxxx Bergeron Plot

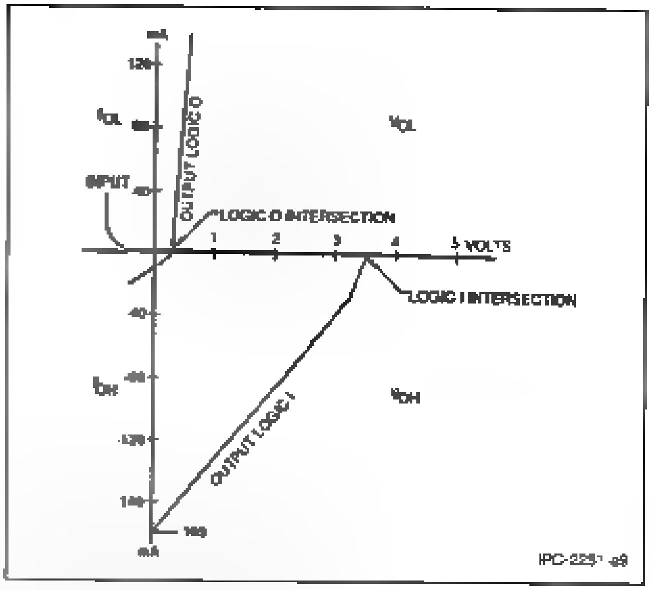


Figure A9 74F24x Bergeron Plot

A.1.3 74Fxxx Power Dissipation

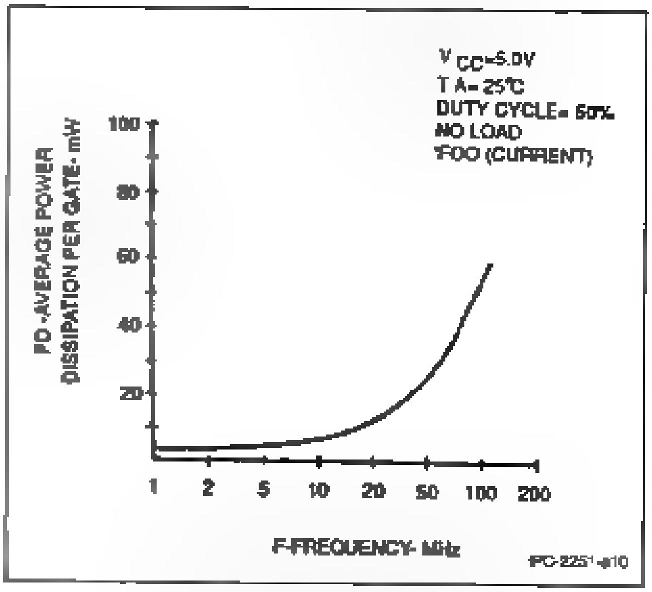


Figure A10 74Fxxx Dissipation vs. Frequency

A.2 74Sxxx Schottky TTL is faster, dissipates more power than 74Fxxx. These are bipolar devices packaged in DIP and SM packages.

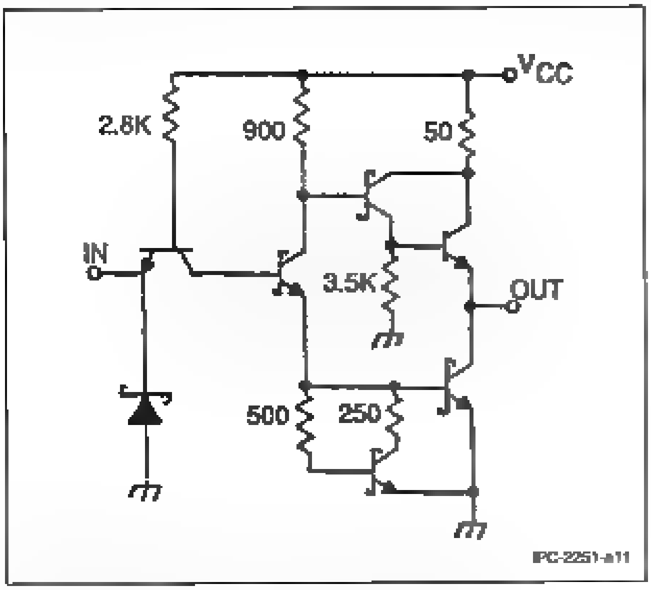


Figure A11 Schottky TTL Inverter Structure

A.2.1 74Sxxx DC Characteristics

The typical data presented in Table A.2 is for Vcc = 5.0V ±5% and Ta = 0 to 70°C.

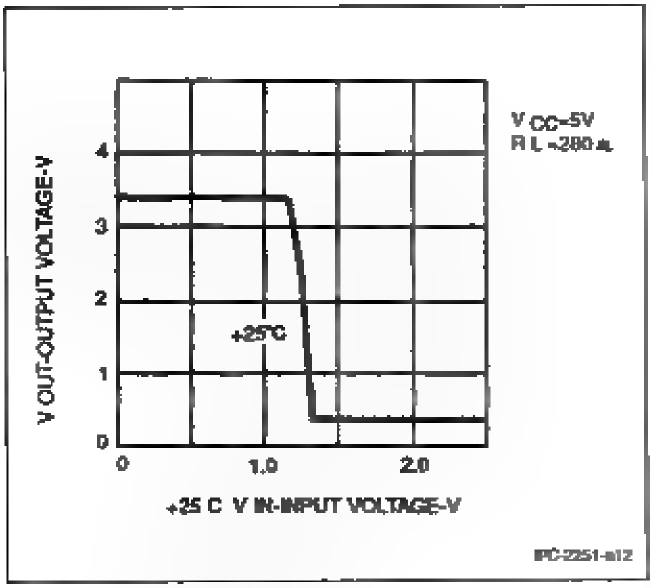


Figure A12 74Sxxx V_o vs V_I

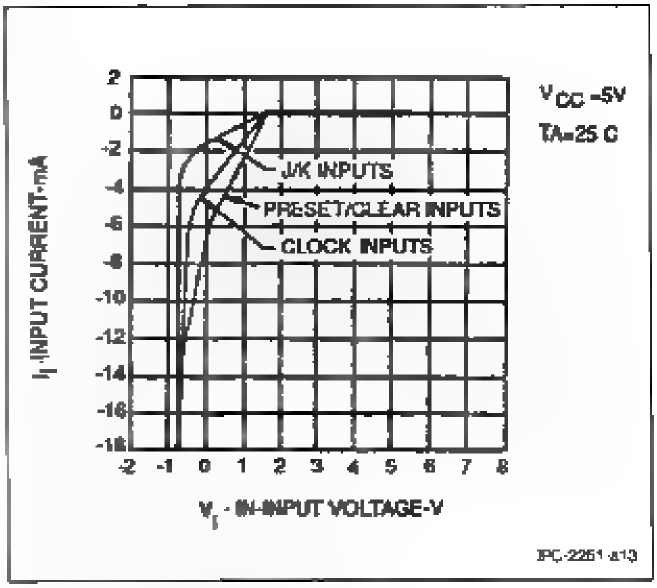


Figure A13 74Sxxx V_I vs I_I

Table A2 74Sxxx Family Characteristics

	Parameter	*Value*	*Units*
VIM	MIN Input HIGH Voltage	2.0	Volts
VIL	MAX Input LOW Voltage	0.8	Volts
VOH	MIN Output HIGH Voltage	2.7	Volts
VOL	MAX Output LOW Voltage	0.5	Volts
IOH	MAX Output HIGH Current	–1.0	mA
IOL	MAX Output LOW Current	20	mA
IIH	MAX Input HIGH Current	50	uA
IIL	MAX Input LOW Current	–2.0	mA
IOZH	MAX 3S HIGH OFF Current	50	uA
IOZL	MAX 3S LOW OFF Current	–50	uA
IOS	MAX Output Short Current	–100	mA
KyHL	HL Capacitive Drive	0.03	ns/pf
KyLH	LH Capacitive Drive	0.05	ns/pf
ICCL	Supply Current, LOW	9.0	mA
ICCH	Supply Current, HIGH	4.0	mA
TpLH	LH Propagation Time	4.5	ns (p 15 pf)
TpHL	HL Propagation Time	5.0	ns (p 15 pf)
NMH	Noise Margin HIGH	700	mV
NML	Noise Margin LOW	300	mV
FOH	Fanout HIGH	20	
FOL	Fanout LOW	10	
Tr	10– 90% Rise Time (Typ)	3.5	nS
Tf	90– 10% Fall Time (Typ)	2.0	nS
Zom	Line Impedance MIN	50	ohms
C1	Max Input Capacitance	5.0	pf

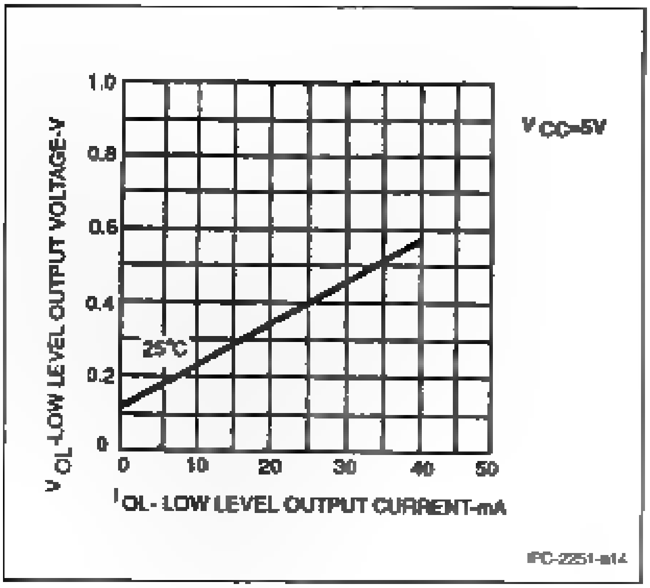


Figure A14 74Sxxx V_{ol} vs. I_{ol}

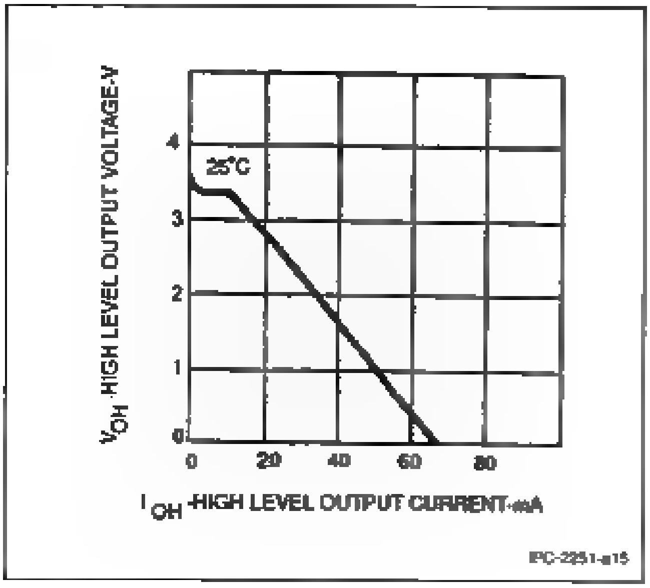


Figure A15 74Sxxx V_{oh} vs. I_{oh}

A.2.2 74Sxxx AC Characteristics

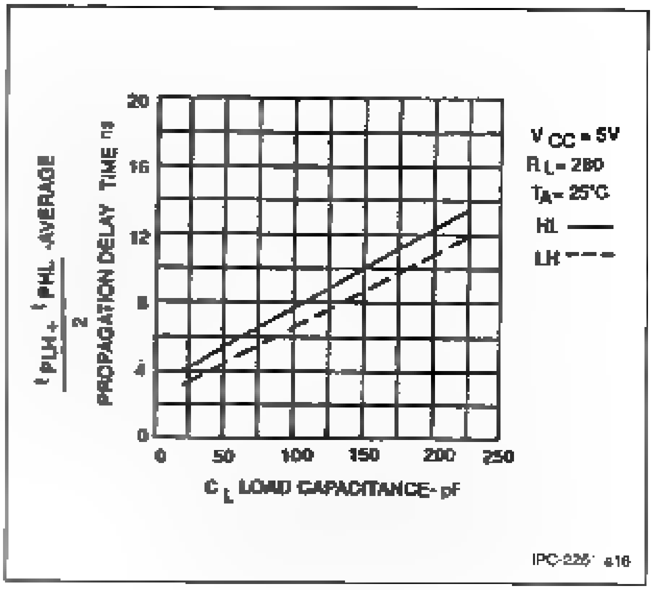


Figure A16 74Sxxx Propagation Delay vs. Load Capacitance

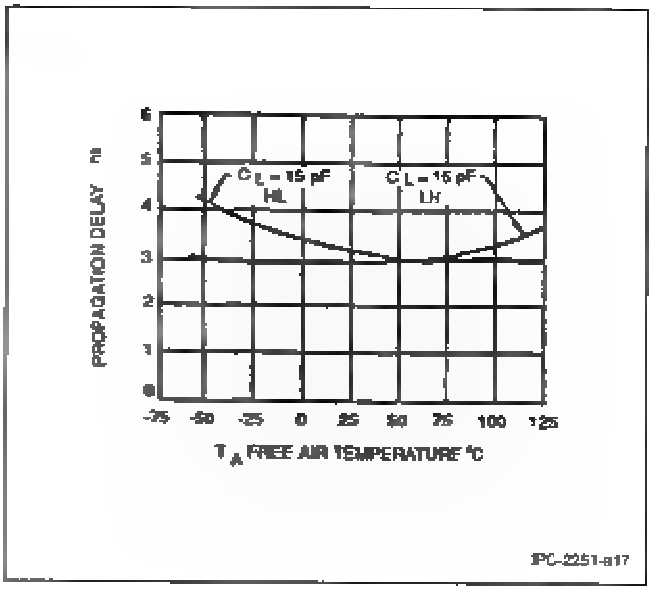


Figure A17 74Sxxx Propagation Delay vs. Temperature

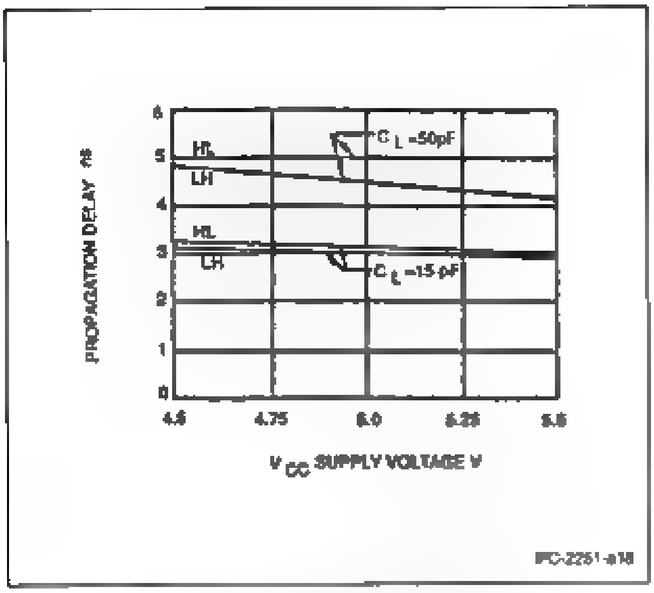


Figure A18 74Sxxx Propagation Delay vs. Vcc

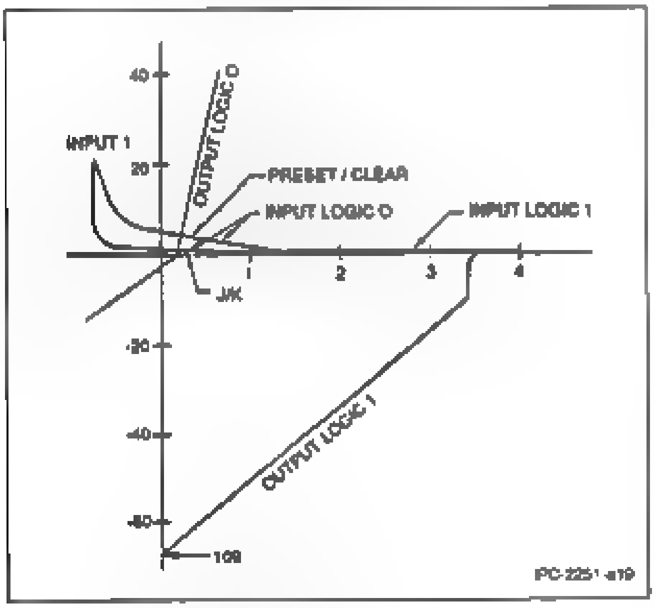


Figure A19 74Sxxx Bergeron Plot

A.2.3 74Sxxx Power Dissipation

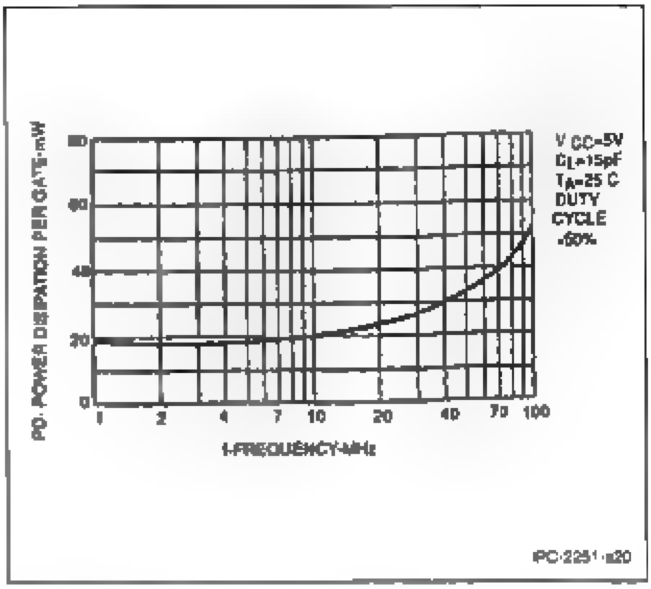


Figure A20 74Sxxx Power Dissipation vs. Frequency

A.3 74ASxxx Advanced Schottky TTL (AS) is faster, dissipates more power, has a higher, more tightly controlled threshold voltage, lower input current, higher output current and lower input and output capacitance than Schottky TTL. These are bipolar devices packaged in DIP and SM packages.

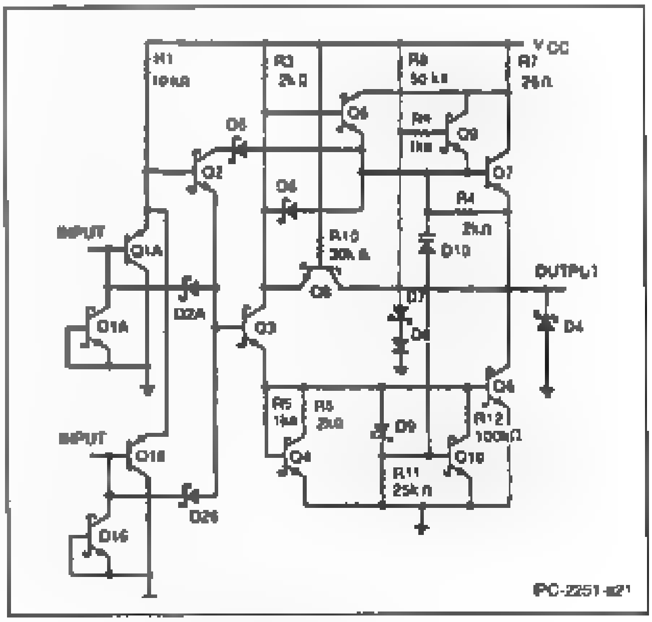

V CC
R1
10kΩ
R3
2kΩ
R6
50 kΩ
R7
78Ω
Q6
Q5
R8
1kΩ
Q9
Q2
Q7
D6
R4
2kΩ
INPUT
Q1A
R10
30k Ω
D10
OUTPUT
Q8
D2A
D7
D1A
Q3
D4
D8
Q4
R5
1kΩ
R6
2kΩ
D9
R12
100kΩ
INPUT
Q1B
Q4
Q10
R11
25k Ω
D2B
D1B
IPC-2251-a21

Figure A21 AS Inverter Structure

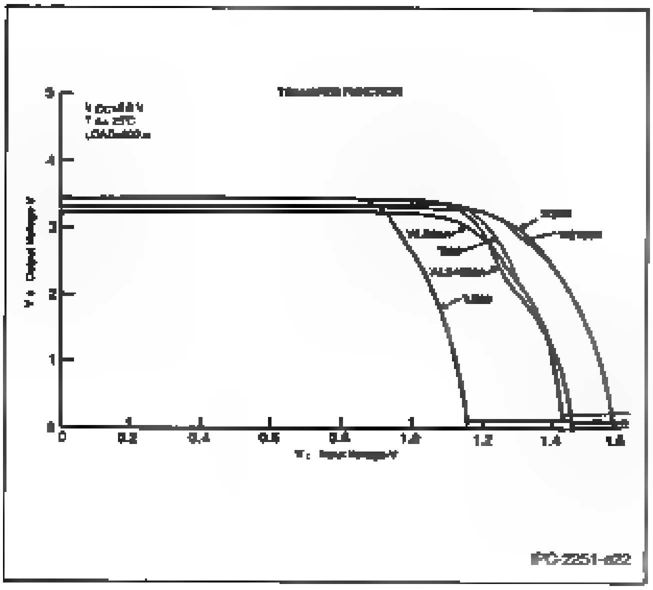


Figure A22 74ASxxx V_o vs. V_i

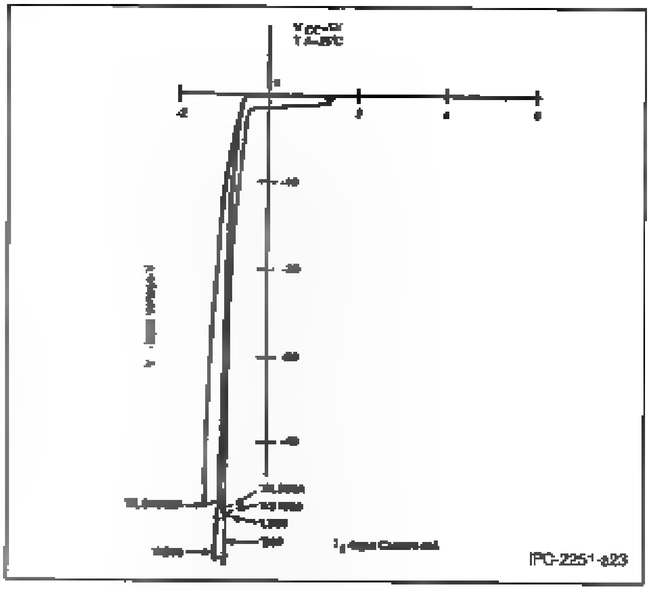


Figure A23 74ASxxx V_i vs. I_i

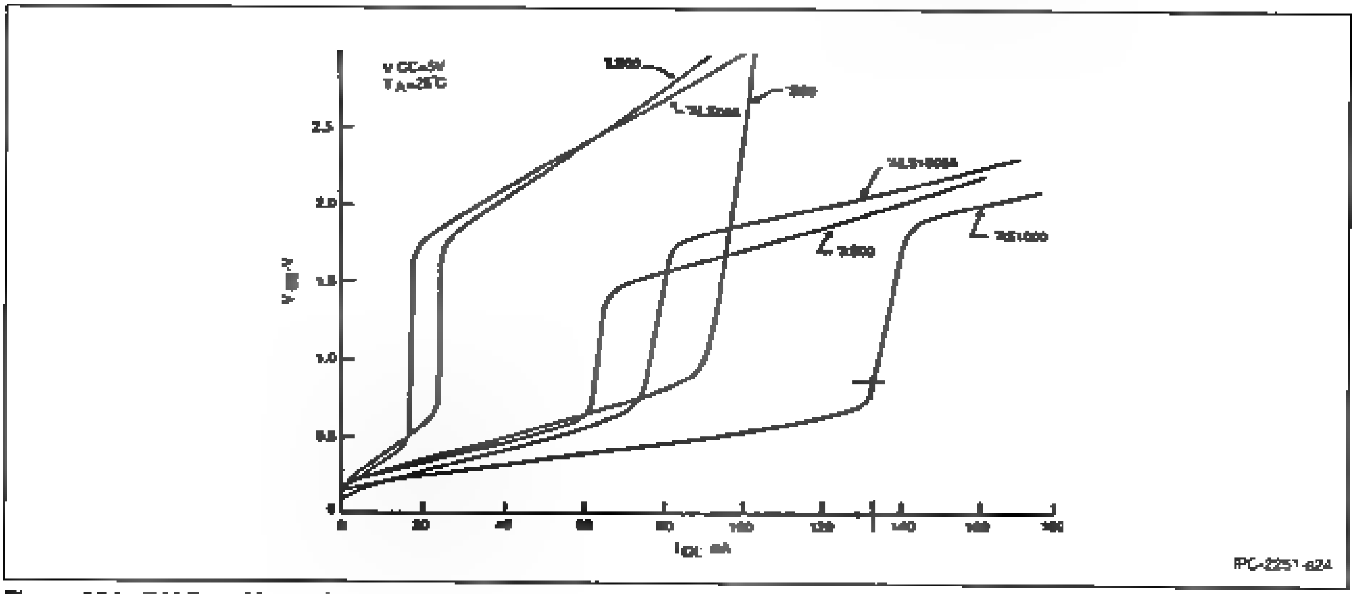


Figure A24 74ASxxx V_{ol} vs. I_{ol}

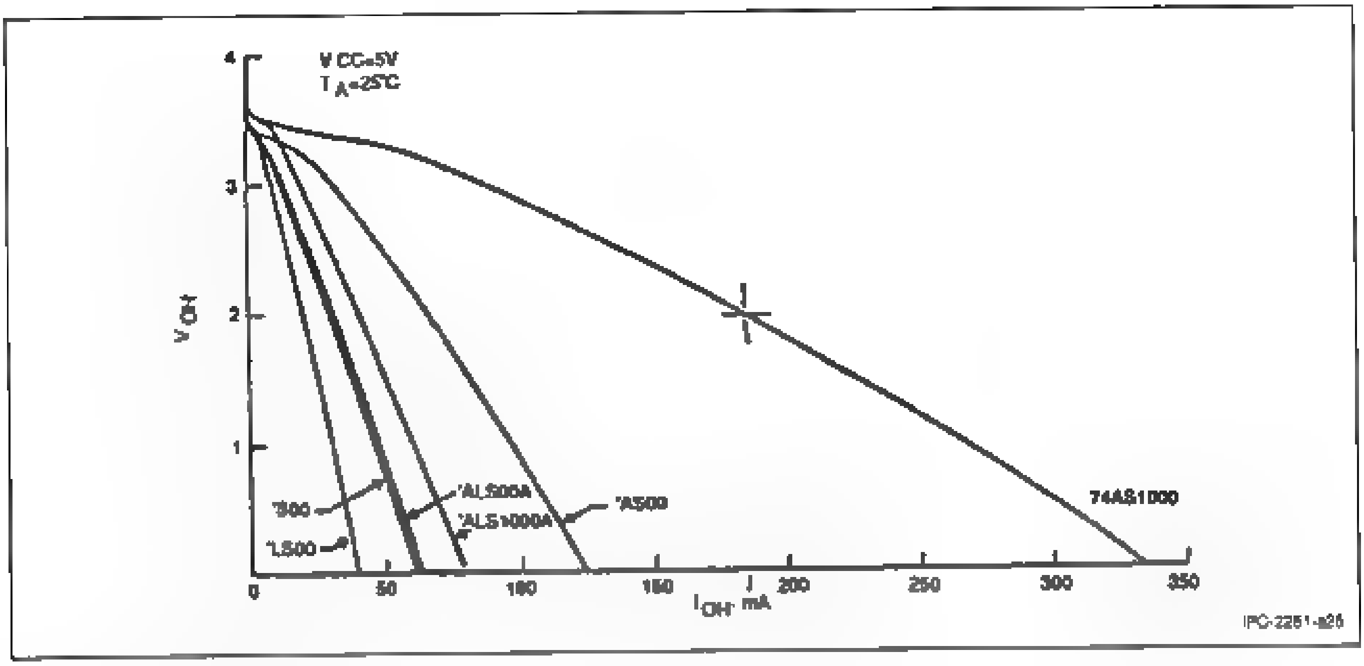


Figure A25 74ASxxx V_{oh} vs. I_{oh}

A.3.2 74ASxxx AC Characteristics

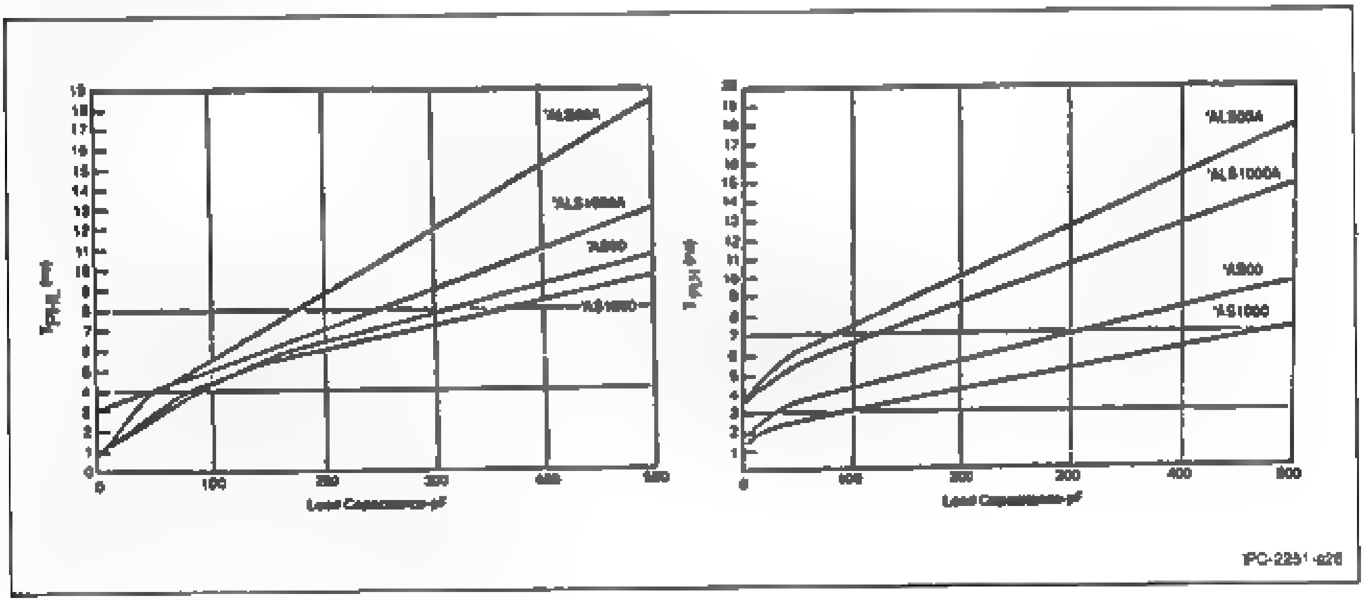
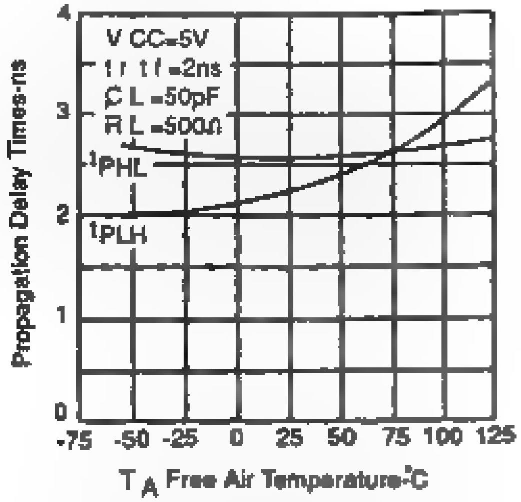
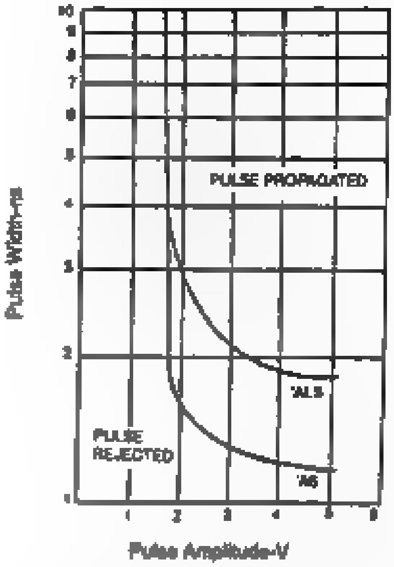


Figure A26 74ASxxx Propagation Delay vs. Load Capacitance



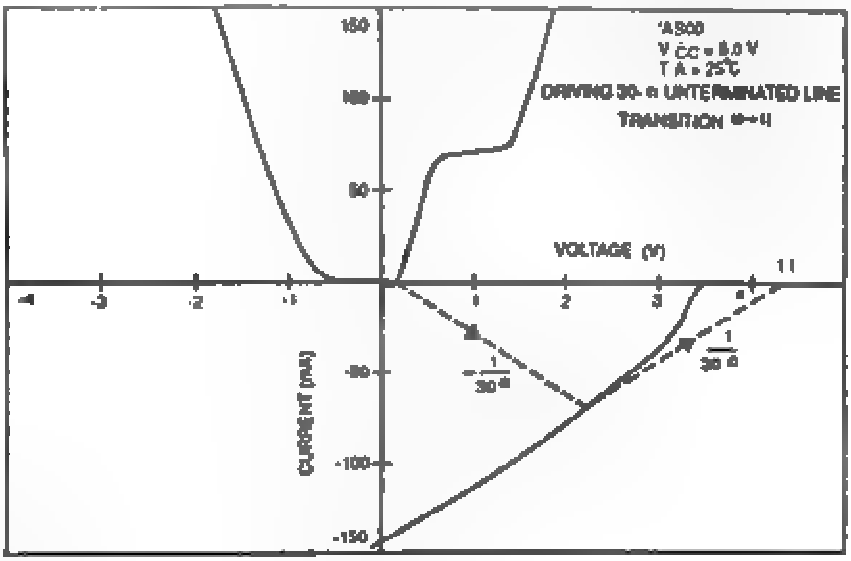
IPC-2251-a27

Figure A27 74ASxxx Propagation Delay vs. Temperature



IPC-2251-a29

Figure A29 74ASxxx Noise Immunity



IPC-2251-a28

Figure A28 74ASxxx Bergeron Plot

A.3.3 74ASxxx Power Dissipation

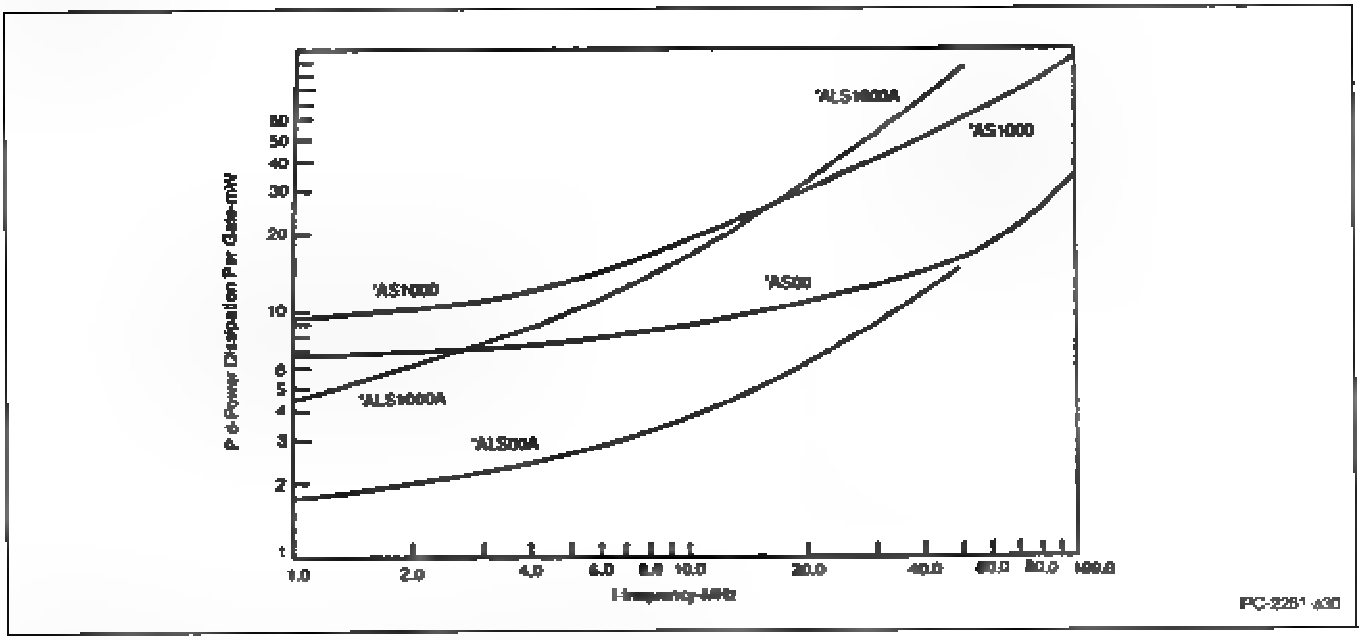


Figure A30 74ASxxx Power Dissipation vs. Frequency

A.4 74LSxxx Low power Schottky TTL (LS) is slower-faster, dissipates less power than 74Sxxx. These are bipolar devices packaged in DIP and SM packages.

A.4.1 74LSxxx DC Characteristics

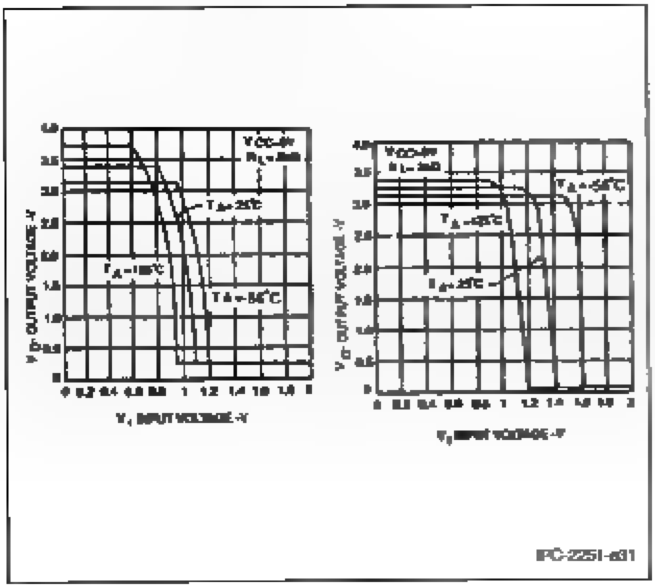


Figure A31 74LSxxx V_o vs. V_i

A.4.2 74LSxxx AC Characteristics

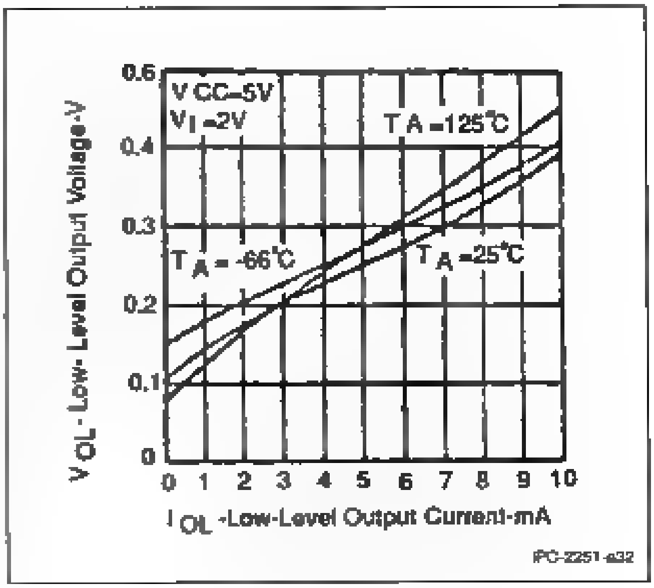


Figure A32 74LSxxx V_{ol} vs. I_{ol}

A.4.2 74LSxxx AC Characteristics

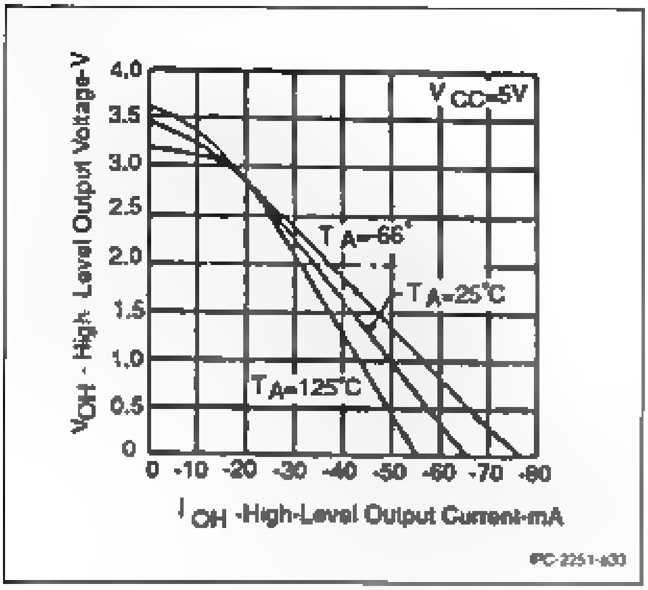


Figure A33 74LSxxx V_{oh} vs. I_{oh}

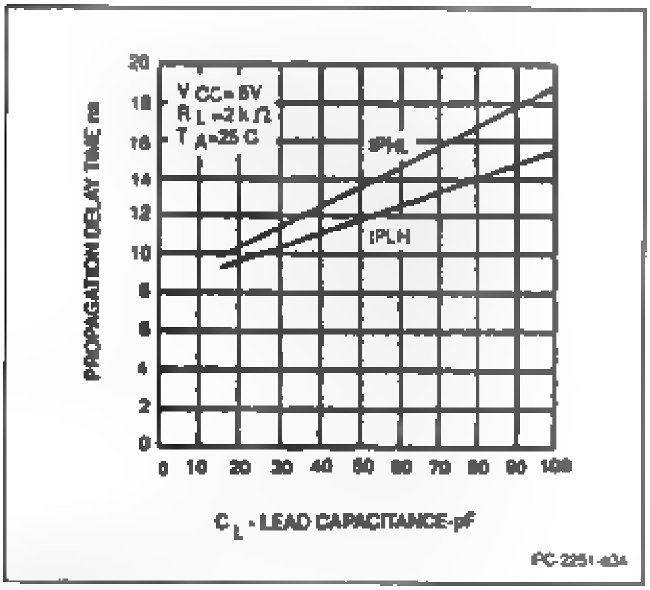


Figure A34 74LSxxx Propagation Delay vs. Load Capacitance

A.4.3 74LSxxx Power Dissipation

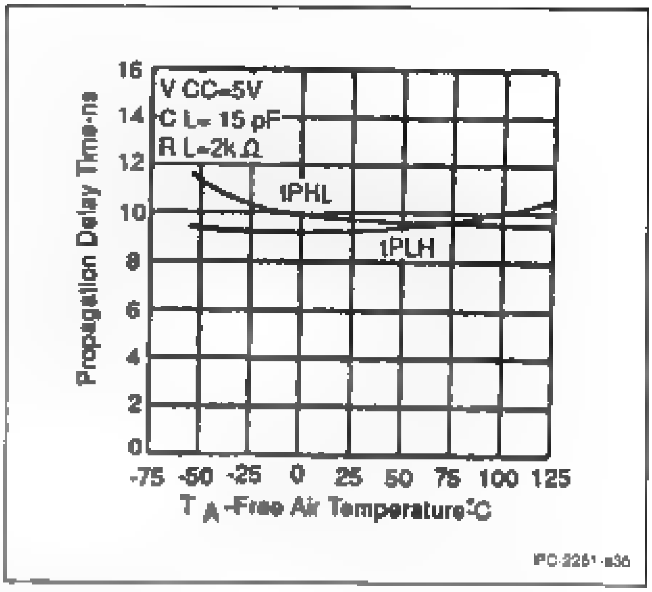


Figure A35 74LSxxx Propagation Delay vs. Temperature

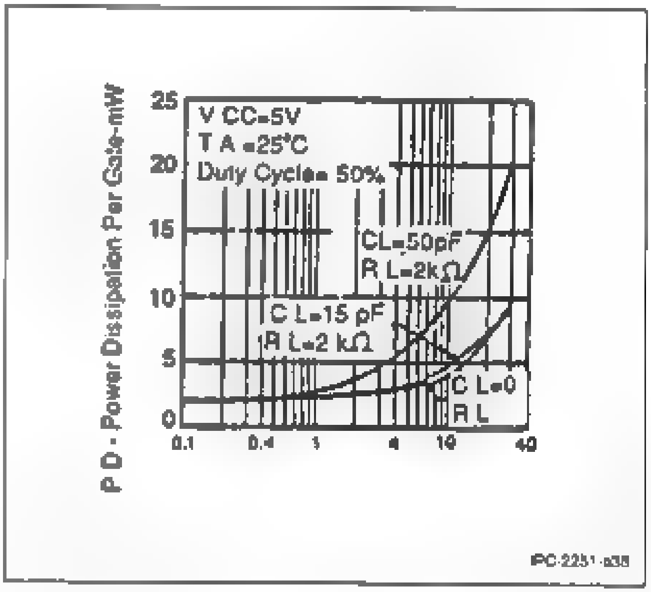


Figure A36 74LSxxx Power Dissipation vs. Frequency

A.5 74ALSxxx Advanced Low Power Schottky TTL (ALS) is faster, dissipates less power, and lower input and output capacitance than Low Power Schottky TTL. These are bipolar devices packaged in DIP and SM packages.

A.5.1 74ALSxxx DC Characteristics

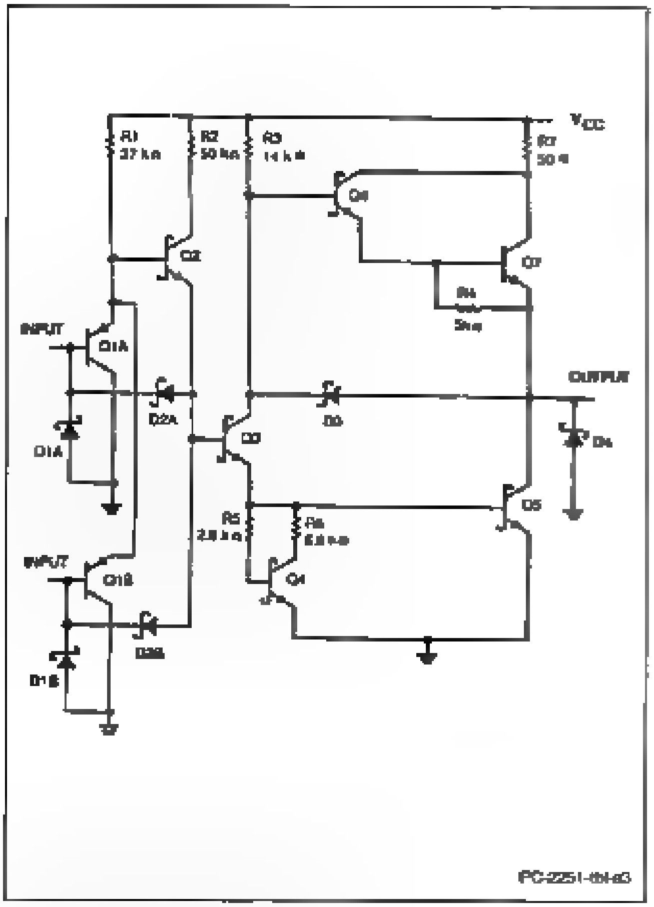

V_{CC}
R1
37 kΩ
R2
50 kΩ
R3
14 kΩ
R7
50 Ω
Q6
Q2
Q7
R4
5kΩ
INPUT
Q1A
OUTPUT
D2A
D3
D1A
Q3
D4
Q5
R5
2.8 kΩ
R6
6.8 kΩ
INPUT
Q1B
Q4
D2B
D1B
IPC-2251-tbl-a3

Table A3 74ALSxxx Family Characteristics

The typical data presented above is for the Vcc = 5.0 V ± 5% and Ta = 0 to 70 °C.

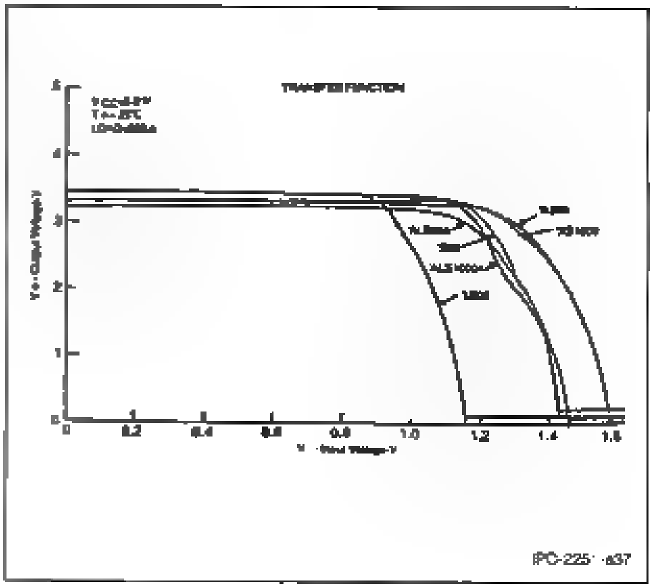


Figure A37 74ALSxxx V_o vs. V_i

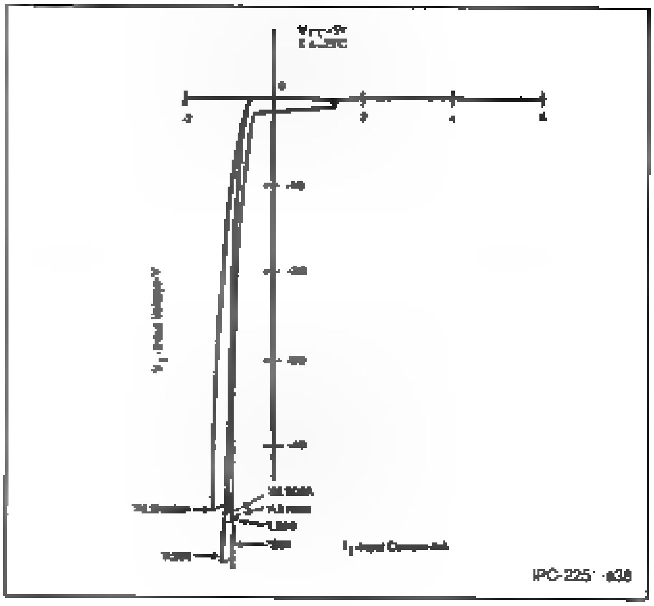


Figure A38 74ALSxxx V_{in} vs. I_i

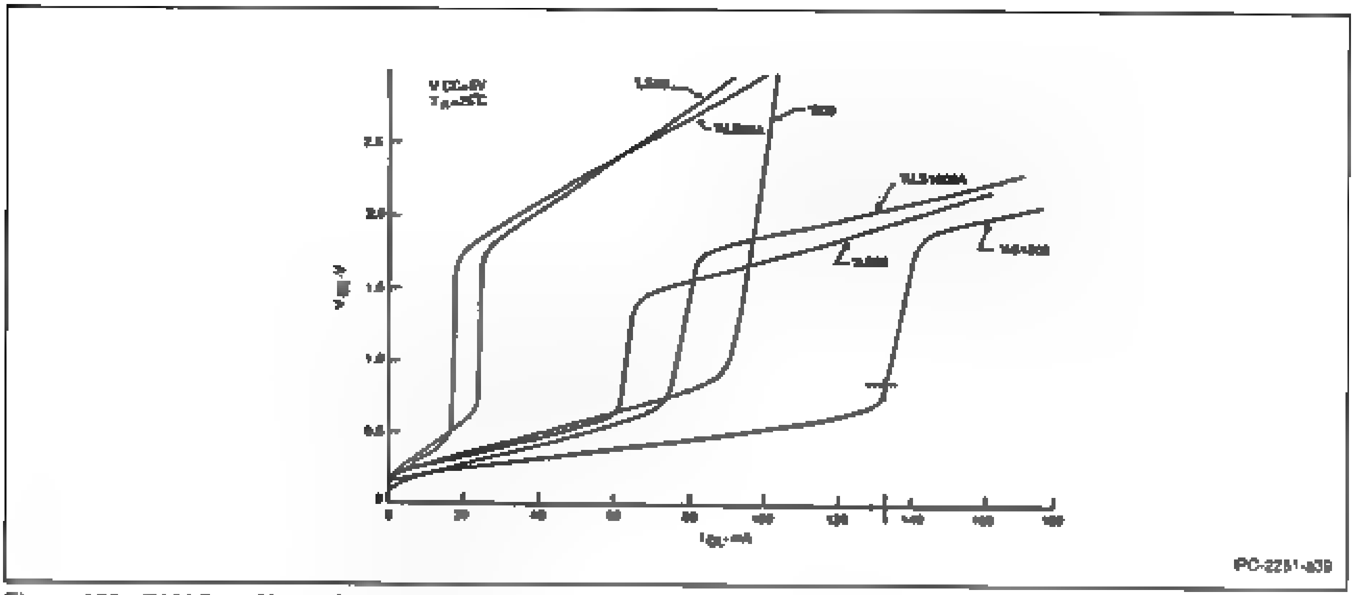


Figure A39 74ALSxxx V_{ol} vs. I_{ol}

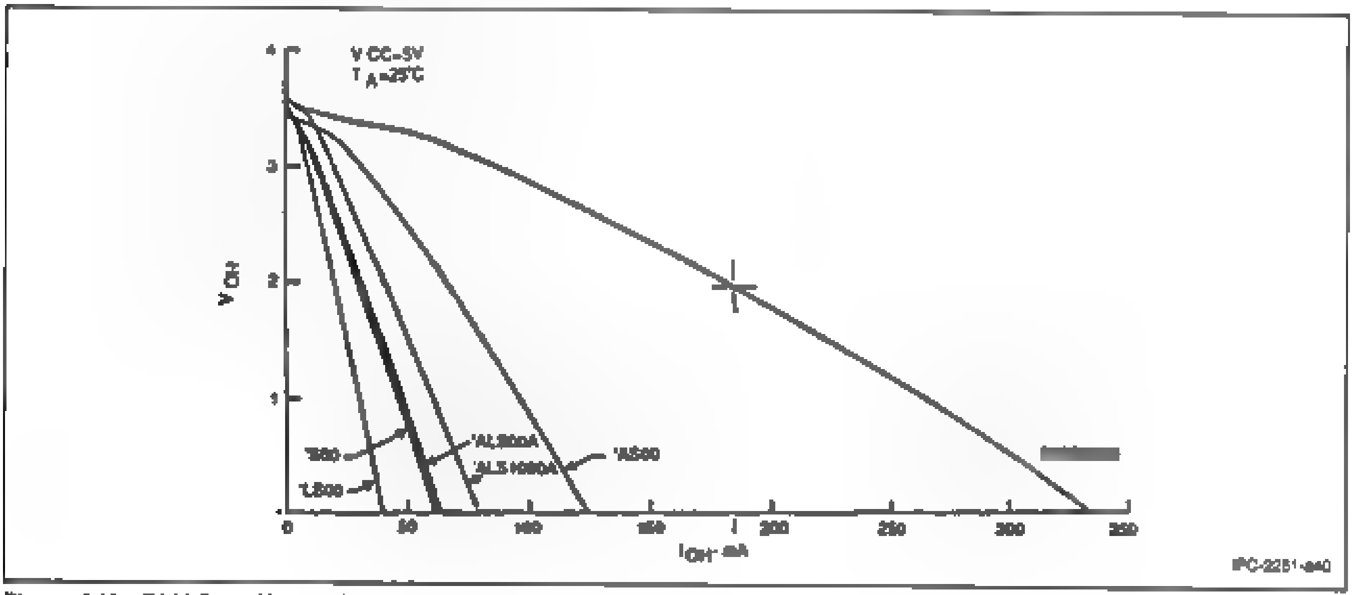
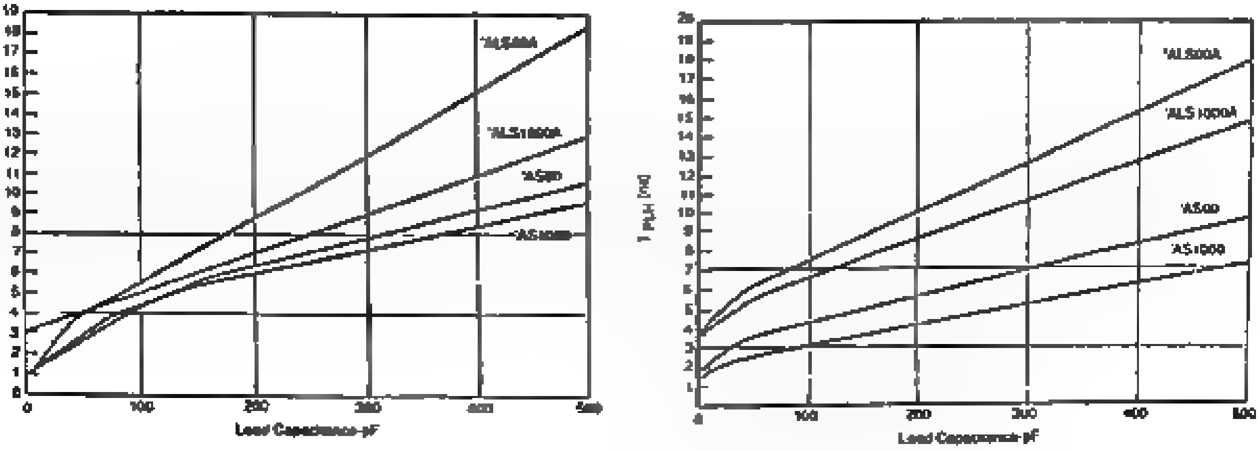


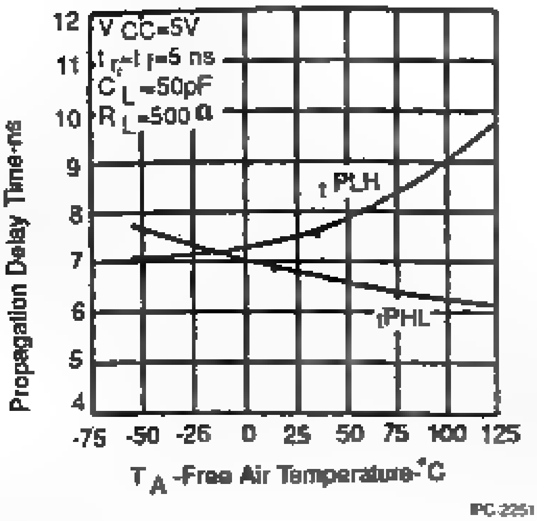
Figure A40 74ALSxxx V_{oh} vs. I_{oh}

A.5.2 74ALSxxx AC Characteristics



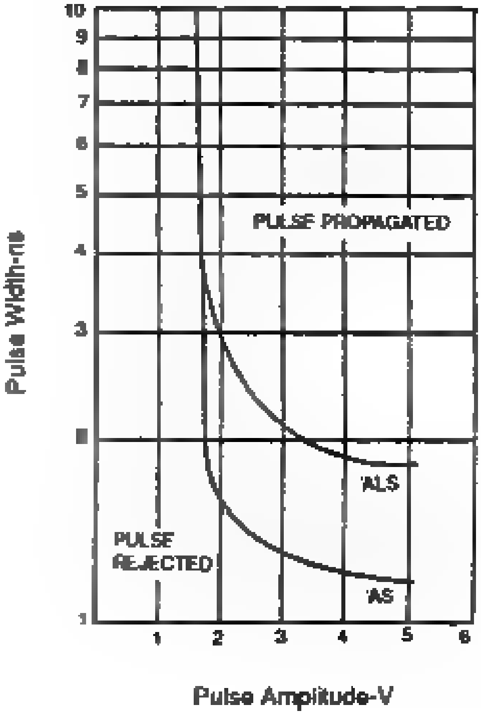
IPC 2251-a41

Figure A41 74ALSxxx Propagation Delay Vs. Load Capacitance



IPC-2251-a42

Figure A42 74ALSxxx Propagation Delay vs. Temperature



IPC-2251-a43

Figure A43 74ALSxxx Noise Immunity

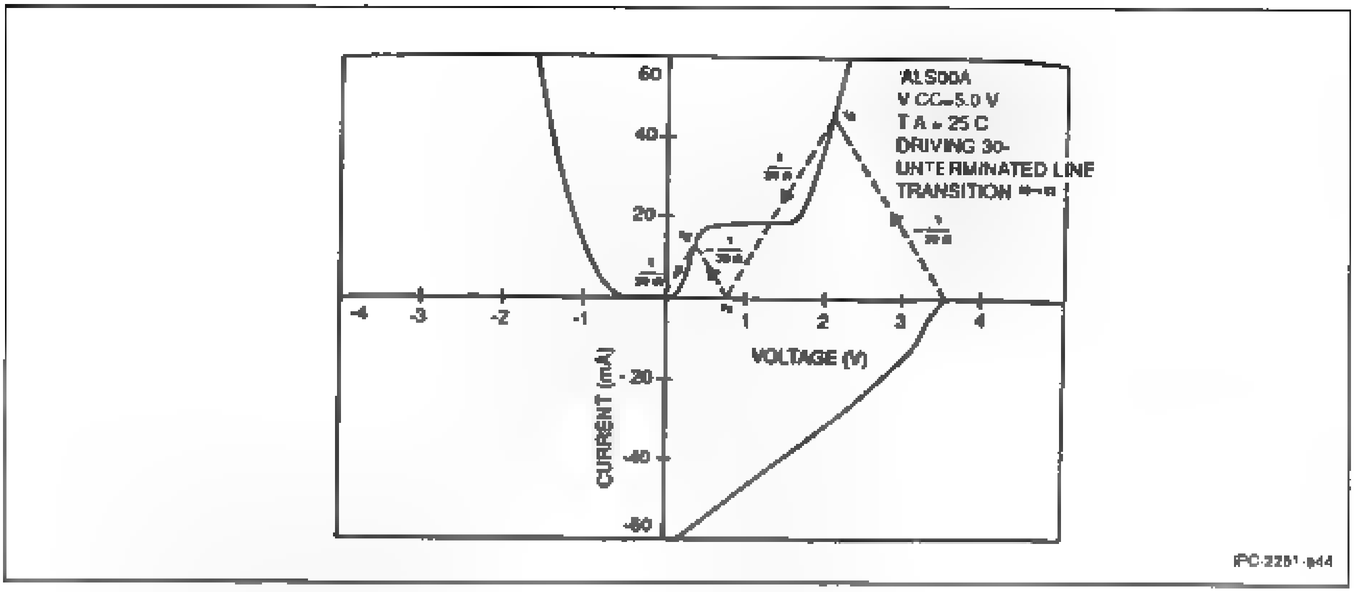


Figure A44 74ALSxxx Bergeron Plot

A.5.3 74ALSxxx Power Dissipation

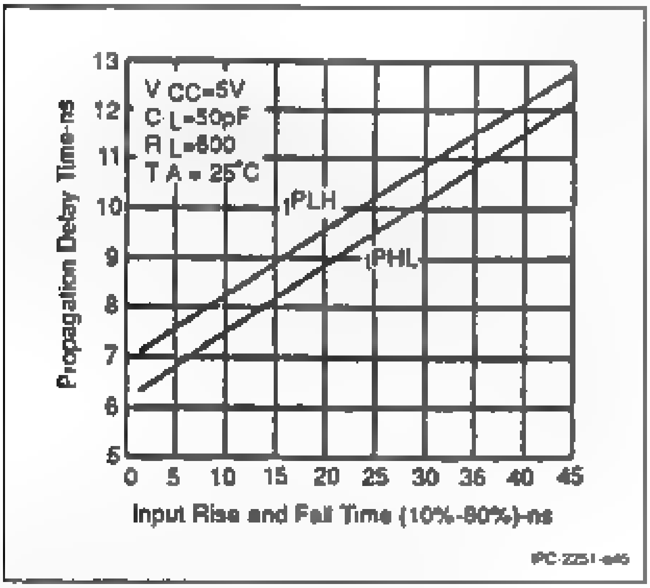


Figure A45 74ALSxxx V_{pd} vs. T_r

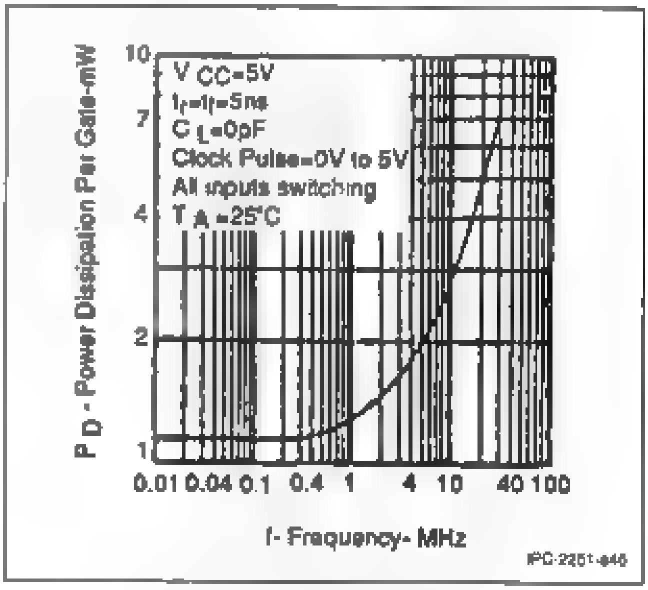


Figure A46 74ALSxxx Power Dissipation vs. Frequency

[illegible]

A.6.1 CMOS DC Characteristics

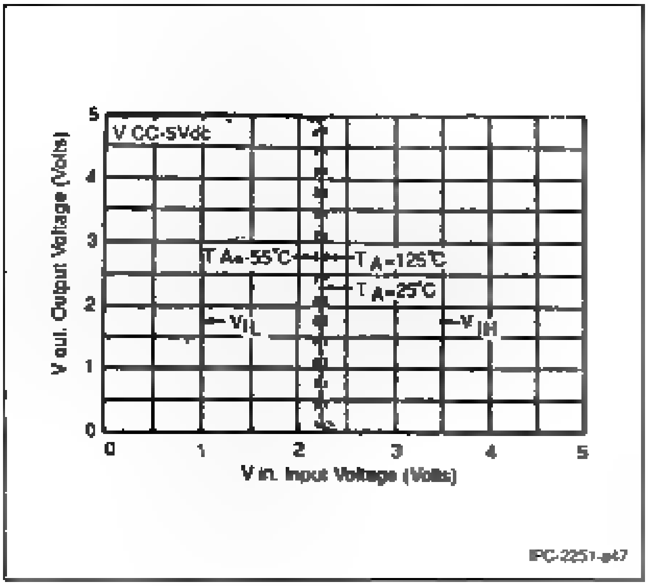


Figure A47 CMOS V_o vs. V_i

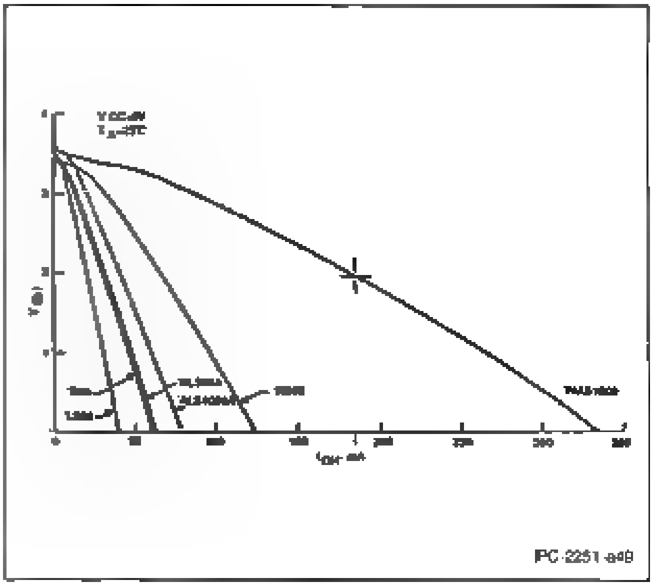


Figure A49 CMOS V_{oh} vs. I_{oh}

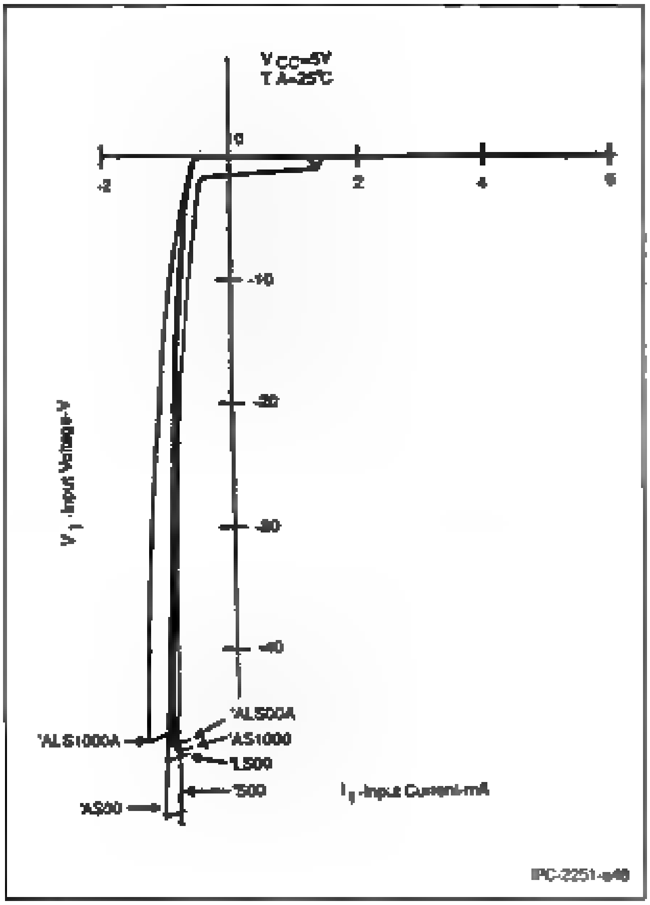
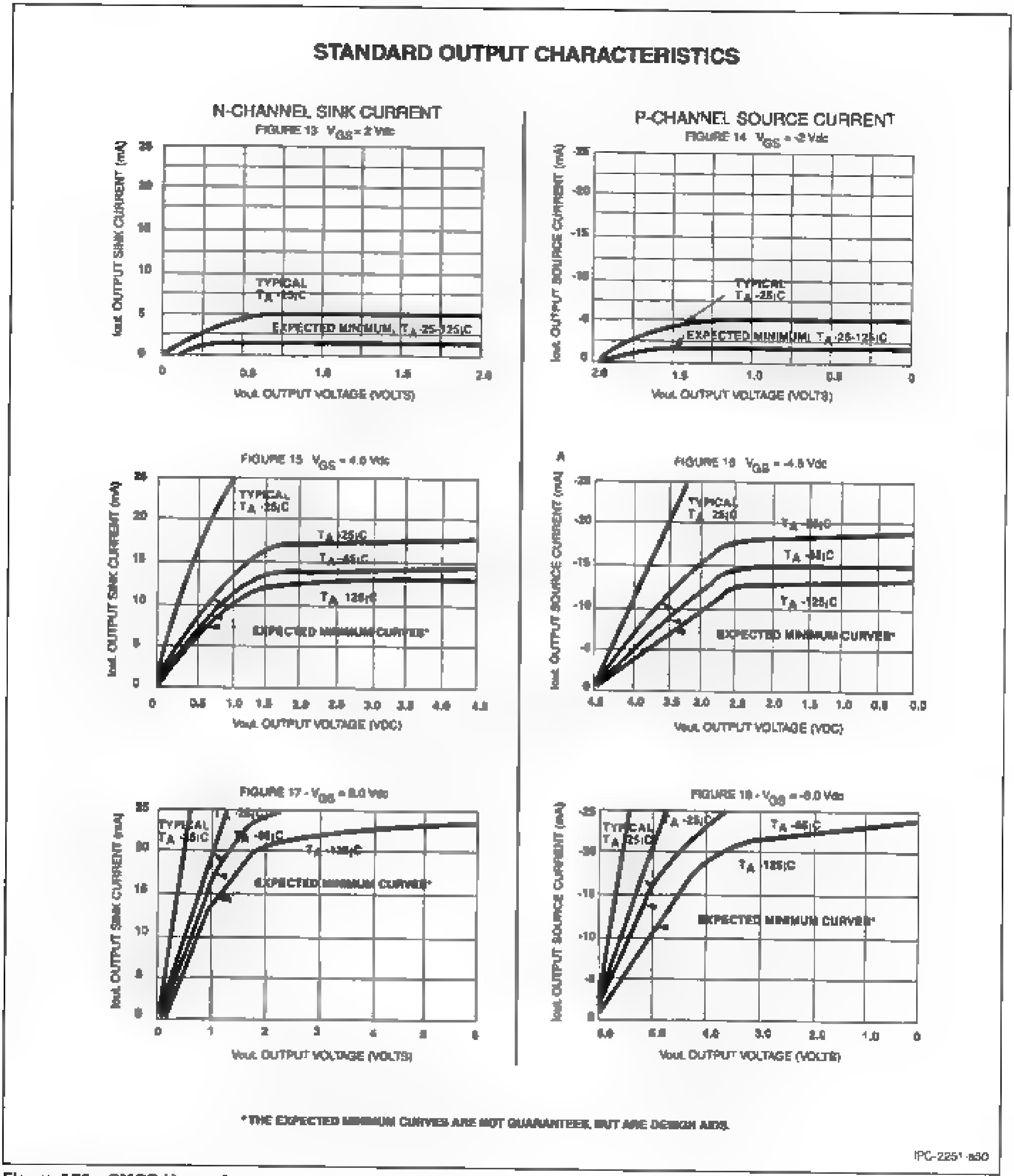


Figure A48 CMOS V_i vs. I_i



* THE EXPECTED MINIMUM CURVES ARE NOT GUARANTEED, BUT ARE DESIGN AIDS.

Figure A50 CMOS V_{ol} vs. I_{ol}

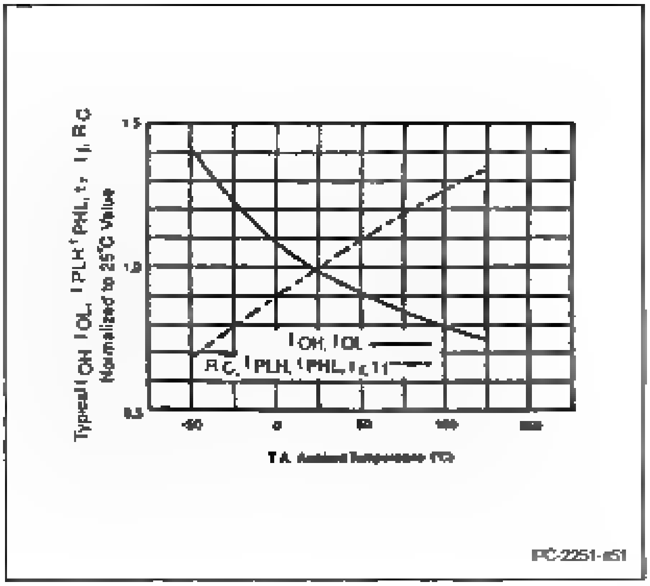


Figure A51 CMOS I_{cl} vs. Temperature

A.6.2 CMOS AC Characteristics

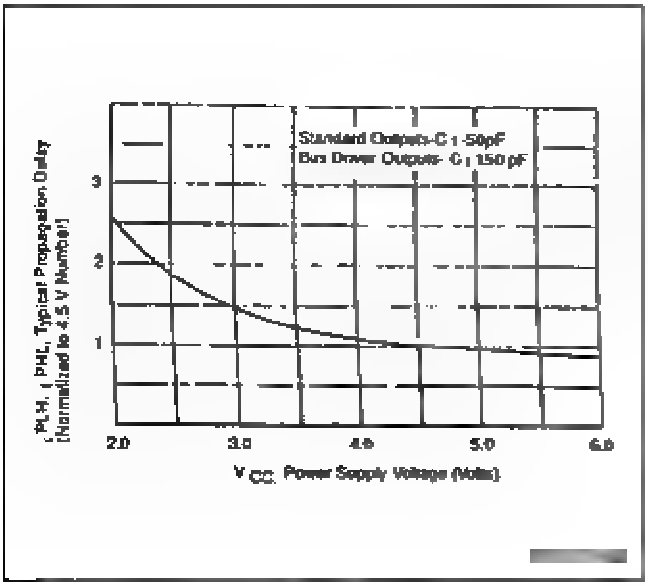


Figure A52 CMOS Propagation Delay vs. Vcc

A.6.3 CMOS Power Dissipation

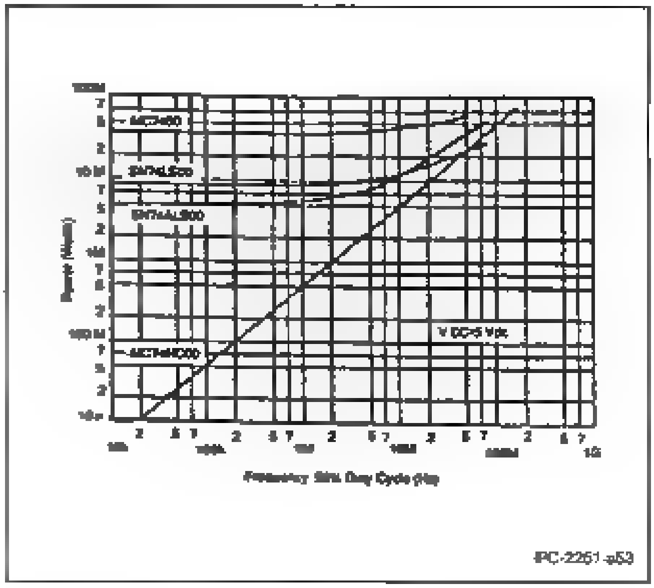


Figure A53 CMOS Power Dissipation vs. Frequency

A.7 10K ECL Emitter Coupled Logic (ECL) keeps the signal in the linear operating region. The signal transition rates are similar to 74Sxxx, but the pulse height is only 600 mV. This logic has fast propagation times and consumes more power than 74Sxxx. 10K ECL is typically slower than 100K ECL. These are bipolar devices packaged in DIP and SM Packages.

A.7.1 10Kxxx DC Characteristics

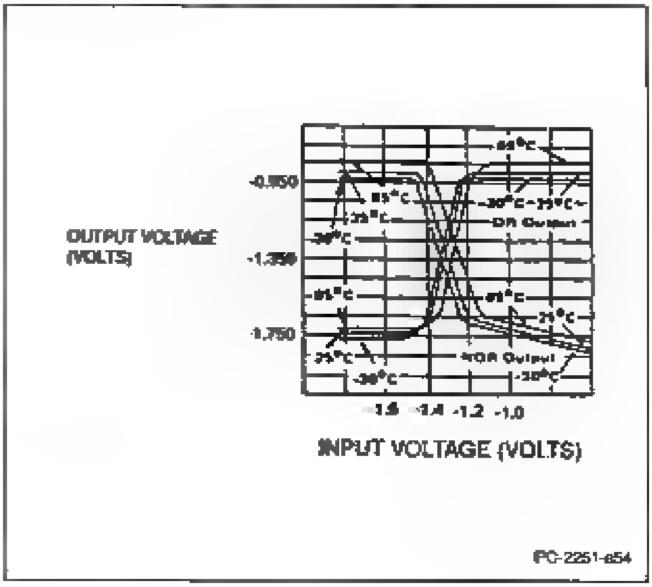
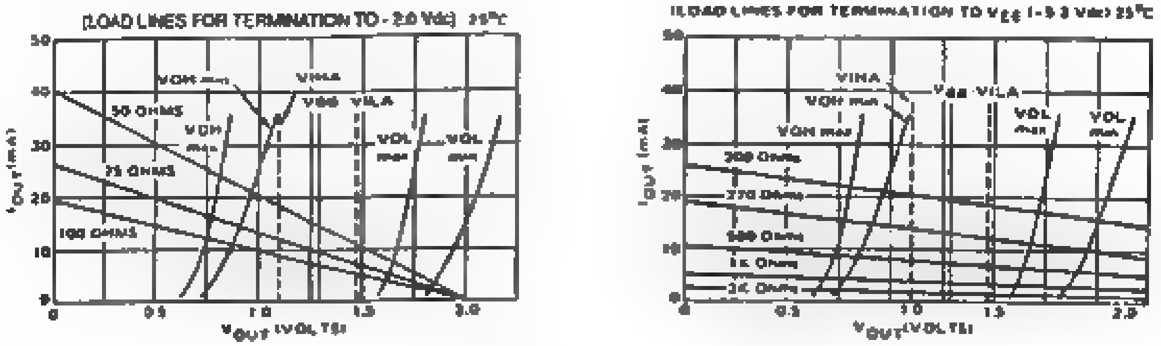


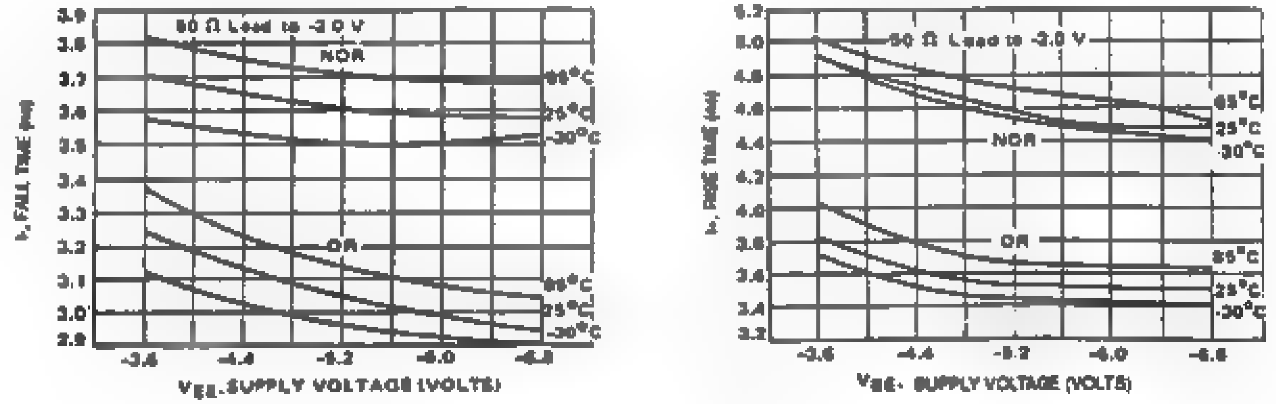
Figure A54 10Kxxx V_o vs. V_i



IPC-2251-a55

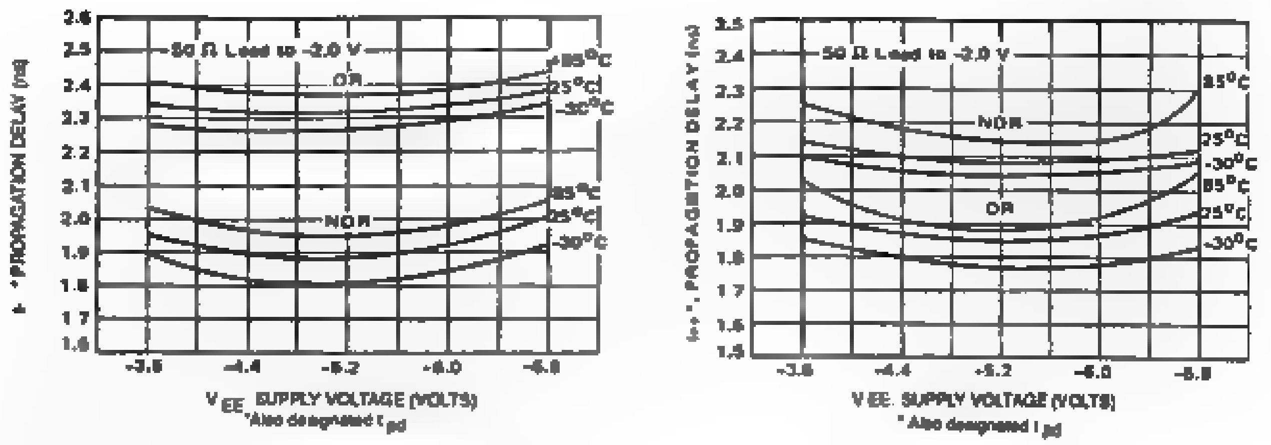
Figure A55 10Kxxx V_{ol} vs. I_{ol}

A.7.2 10Kxxx AC Characteristics



IPC-2251-a56

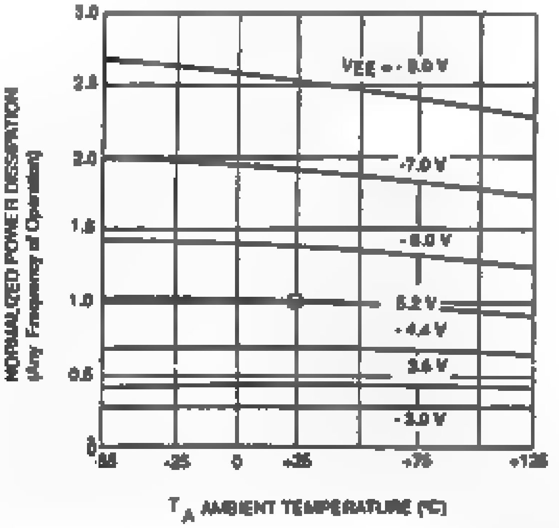
Figure A56 10Kxxx Propagation Delay vs. Input Risetime



IPC-2251-a57

Figure A57 10Kxxx Propagation Delay vs. Temperature

A.7.3 10Kxxx Power Dissipation



IPC-2251-a58

Figure A58 10Kxxx Power Dissipation vs. Temperature and V_{EE}

A.8 100Kxxx Emitter Coupled Logic (ECL) keeps the signal in the linear operating region. The signal transition rates are faster than 10K, but the pulse height is only 400mV. This logic has fast propagation times and consumes more power than 10KECL. 100K ECL is typically faster than 10K ECL. These are bipolar devices packaged in DIP and SM packages.

A.2.1 100Kxxx DC Characteristics

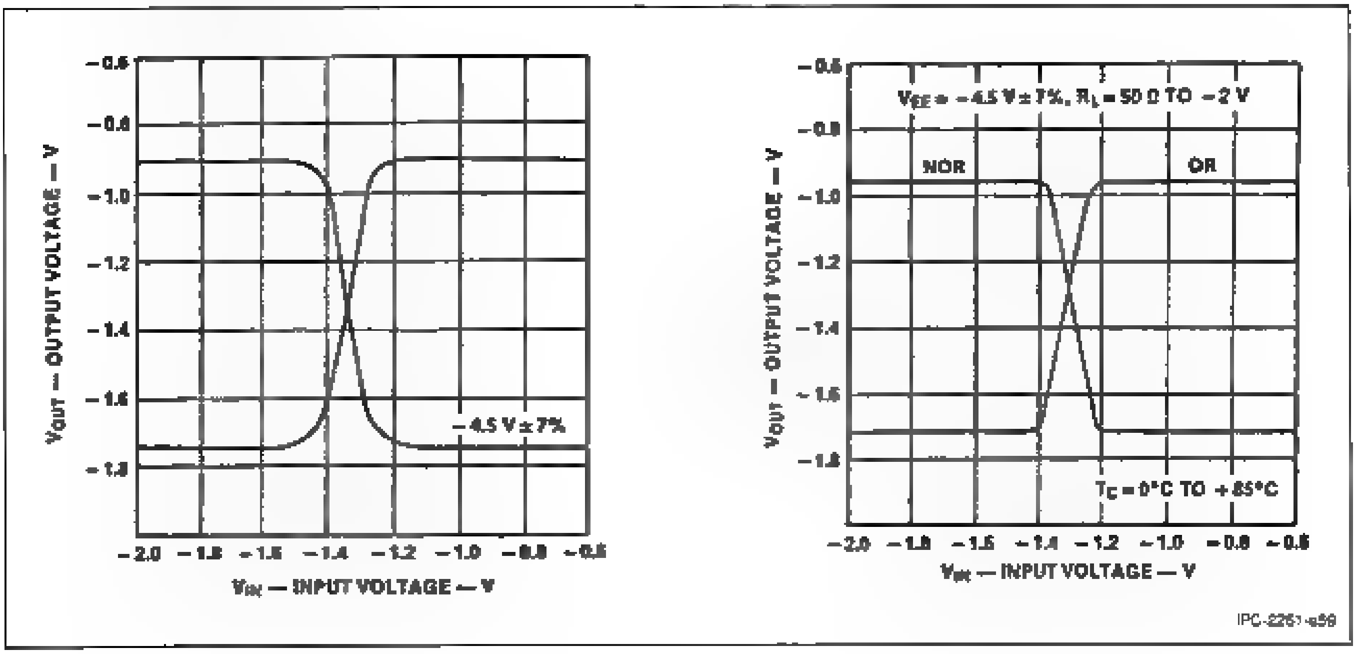


Figure A59 100Kxxx V_o vs. V_i

Appendix B

TUTORIAL

B.0 System Electrical Design Concepts

B.1 Electromagnetic Wave Signals Propagation Versus Electric Current In Conductors Interconnection and the packaging of electronic components primarily have been the domain of mechanical designers who were concerned with such factors as weight, volume, power, cooling, form factor and environmental constraints, with interconnections specified in wire listing or to/from listings. Conductors of electrical signals were routed with only two concerns: that continuity was maintained between points and that no shorts were permitted. Aside from providing a good electrical path, the electrical properties of the signal were not a major concern.

However, recent advances in digital integrated circuits have introduced new devices with extremely fast rise times housed in high density microelectronic packages. In order to optimize system performance, these devices require a wiring technology that supports high density interconnection and, at the same time, provides superior electrical performance. With the market's appetite for high speed processing growing at over 30% per year, high speed digital processing is no longer the domain of a few scientific super computers. Even medium size mainframes and minicomputers are touting processing rates of more than 3 million instructions per second (MIPS) and machine clock rates of 50 to 250 MHz, and the high speed technology has penetrated the commercial, telecommunications and military markets.

While many system problems are associated with high speed digital processing, none has received more attention lately than interconnection. The reason for this attention is shown in Figure B1 where it is evident that as system speeds increase, interconnection and packaging become the bottlenecks that slow system performance. Systems using 100K ECL circuitry have almost 55% of the system delay in the packaging and interconnection. This situation is even worse when GaAs technology is utilized. CMOS is normally considered a "slow" technology, but is now being designed into system clock rates in excess of 100 MHz. In these cases, not only is system delay a problem but signal attenuation becomes an issue with the low powered CMOS devices.

What is the fundamental phenomena that imposes the special treatment for the so called "high speed digital" interconnections? We have come to assume that signal routing and the routing of electrons in the form of current and voltages are synonymous. However, at the higher speeds, more and more energy is propagated as electromagnetic waves. Resistance must now be thought of as resistance to electro-magnetic wave, which is the alternative item for impedance. Instead of voltages and current, we now must think in terms of electric and magnetic fields. The parameter that affects the electric field is called capacitance and that affecting the magnetic field, inductance, but more specifically self-inductance. Self means the value is determined by the conductor itself. On the other hand, capacitance is determined by relationship between conductors and the surrounding medium. Consequently, from the design standpoint, we are designing to specific impedance values by trying to control the capacitance and inductance with line width and thickness variations, dielectric thicknesses, aspect ratios and the relative permittivity of the material between conductors as transmission lines. Signal paths must be kept short to minimize propagation delays. Even if it were possible to make a circuit capable of switching at infinite speed, it would be the interconnection that would dictate the performance of the systems using these devices. Figure B2 illustrates the switching speed of a device (i.e., transistor) vs. propagation delay in a medium commonly used in the printed board industry. This can also be plotted for hybrid ceramic circuits, silicon mother boards and other means of signal transport.

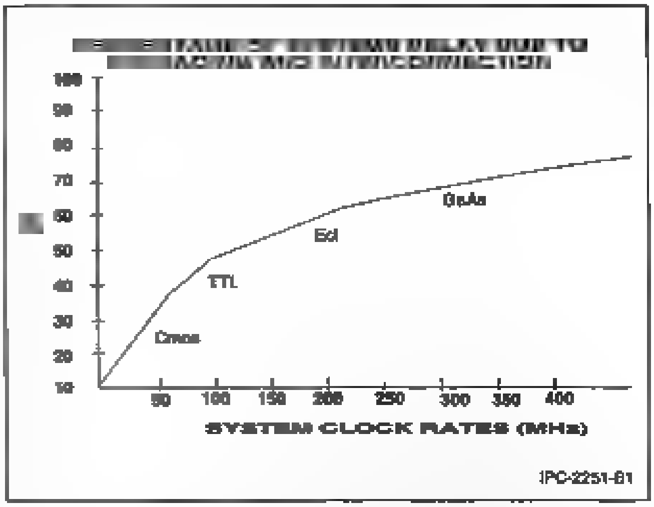


Figure B1 Propagation Delay Due to Packaging Effects

The plot shows the immediate degradation of the device performance due to the limitation of signal propagation delays through a common interconnection medium. Note that the simplest possible system configuration has been assumed, i.e., one flip-flop sending a signal to another. Even under these unrealistically simplified conditions, the two flip-flop system-using devices with infinite switching speeds could not operate any faster than 1 GHz if the signal is transmitted through 6″ of printed board material, 4″ of ceramic or 3″ of silicon. If the switching devices were rated 1 GHz, travel through 6″ of printed board material will cut the speed in half to 500 MHz.

The conclusion of these considerations is that a close interrelationship between mechanical design and electrical performance exists in the case of interconnection lines involving high speed digital signals. This interdependence did not exist or it could be ignored in low speed signal applications and it imposes new design rules, restrictions and process controls.

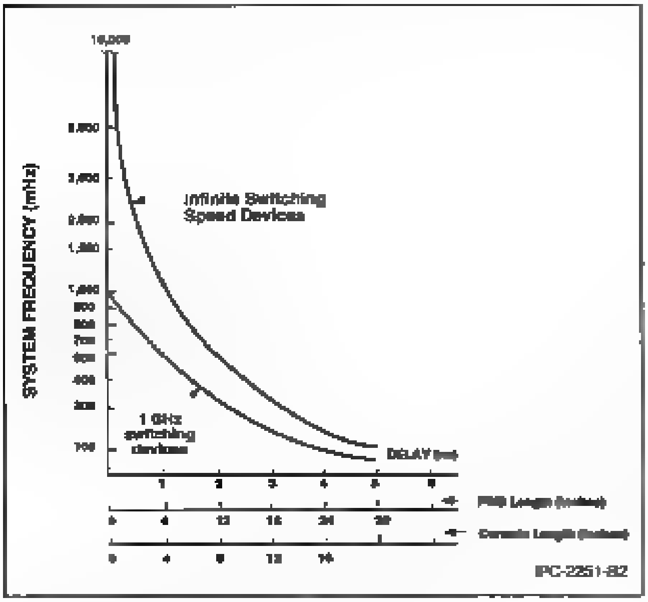


Figure B2 System Speed Vs. Signal Growth Length

To meet the challenges of high speed digital processing, today's circuit board must:

- reduce propagation delay;
- lower crosstalk and other line parasites;
- reduce signal loss; and
- allow high and very high density interconnections.

It is important to mention here that these specific requirements must be accomplished on top of all the other mechanical and electrical specifications as defined for the existing technologies already in use.

To achieve these desired goals the designer must start by controlling the impedance of the transmission lines on the board. For this reason, the circuitry used in high speed digital applications is known under the generic name of "Controlled Impedance Packaging."

B.2 Critical Signal Speed At what frequencies should there be concern about wave propagation rather than just current in conductors? The general rule is that transmission line effects (wave effects) become an important design consideration when the length of the interconnection approaches 1/7 of the wavelength of the signal being transported. If the system clock frequency is 300 MHz, the wavelength in air is about 1 m.

Unfortunately, this is not the frequency of concern. Generally, the system clock is a repetition rate of a square wave pulse. Most systems will be digital and the information as to whether the pulse is a "1" or a "0" is carried in the leading edge of the pulse (the sharp rise). This edge must be permitted to rise (or fall) as quickly as possible. Frequency and the rise time of the signal are related by the relation Tr = 0.35/f where Tr is the rise time in nsec and f is the frequency in GHz.

A method of determining the required rise is to examine the type of devices that need to be interconnected. Table B1 shows the rise times values for some of the most popular high speed ICs.

Table B1 Rise Time

Device Family	Output Pulse Rise Times (nsec)
TTL	6–9
Schottky TTL	2–3
ECL	0.45–0.75
GaAs	0.05–0.20

For example, ECL has a 0.45 rise time with a corresponding frequency of concern of 0.35/0.45 GHz or 777 MHz. This translates to a wavelength in air of about 15″, 7.5″ in FR-4 or less than 4″ in ceramic. This means that for circuit boards fabricated from FR-4, if the interconnection path is more than 1.0″, the electromagnetic properties of the signal, and the waveguide or transmission line effects should be considered.

From this example, it becomes obvious that the critical signal speed is the signal rise/fall time instead of the clock frequency.

B.3 Transmission Line Effects

B.3.1 Signal Propagation Delay It is easy to understand this phenomena if we consider the propagation of an electromagnetic wave through an insulator medium as the model of signal transmission in a "high speed" board. The propagation speed of an electromagnetic wave is related to the permittivity of the insulating medium by the relation $v_p = c/(\varepsilon_r)$, where c is the velocity of light (3×10^8 m/sec) and ε_r is the permittivity of the insulating material. The permittivity of polyimide is about 3.5, glass epoxy for printed board is 4 to 5, hybrid ceramic is 9-10 and that of silicon wafers is about 15. To preserve the speed of high speed devices, we must think in terms of total interconnection lengths.

Generally speaking, one can say that for ECL circuits with terminated lines, the propagation velocity varies inversely with the square root of the line capacitance and for CMOS circuits, where the delay is caused by skew, the speed varies inversely with the capacitance.

B.3.2 Crosstalk Crosstalk is the transfer of energy between adjacent circuits via capacitive or inductive coupling. The energy from the "source" circuit becomes superimposed on the "receptor" circuit signal leading potentially to malfunction of the logic, including spurious switching and circuit dropouts. Figure B3 represents two adjacent uniform signal lines, one of which carries a pulse-type signal. The coupling between the two lines is by mutual inductance and capacitive components L_{12} and C_{12}, respectively. Signals introduced into the active line will be induced into the quiet or passive line by electromagnetic fields that accompany the traveling signal on the active line. The near end refers to the signal originating end, the far end, the signal receiving end. It is assumed that the active and quiet line both have good returns to ground.

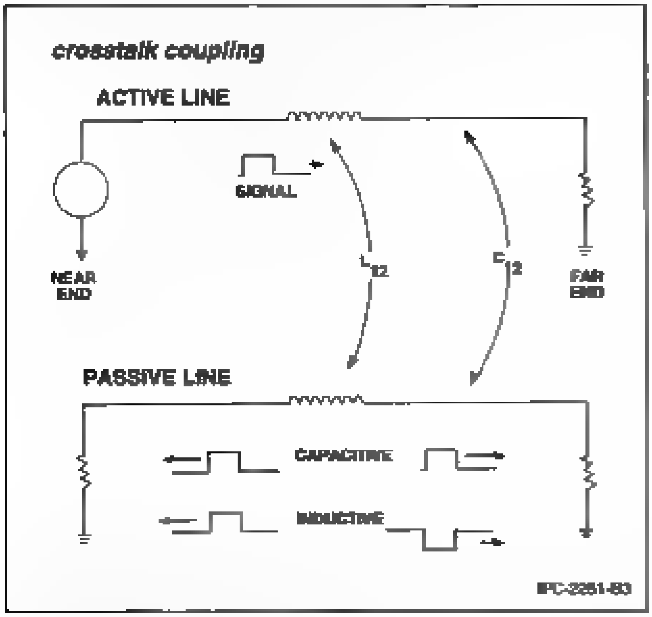


Figure B3 Crosstalk Coupling

If the magnetic coupling is separated from the capacitive coupling between the active and passive lines, different phenomena occur. The coupled signals going toward the far end are called forward crosstalk and the coupled signals in the passive line coming back to the near end are called backward crosstalk. The coupling due to capacitive effects (that due to the electric field) causes a smaller replica of the active signal to be sent to both the far and the near ends, with the same polarity as the active signal.

The coupling due to the inductive effects (that due to the magnetic field) also sends signals to both the near and the far ends, but the signal to the far end is inverted (opposite polarity) to that of the active signal. Consequently, the backward crosstalk composite of the inductive and capacitive coupling is the sum of signals, but the forward crosstalk composite is the difference between the two signals, usually resulting in a smaller component. Therefore, the crosstalk coupling coefficient found in references is different for the two.

The degree of isolation required of crosstalk for systems is usually specified as 60 dB for analogue type signals and 26 dB for digital signals.

The most common techniques of reducing crosstalk effects in high density circuits are as follows:

a) to increase the separation;
b) to reduce the parallel length;
c) to reduce the line impedance;
d) to reduce the signal level;
e) to interspace signal traces with ground trace

B.3.3. Switching Noise When gates are switching, current is either drawn or passed to the power supply through the power/ground links. When this current has high frequency components, the self-inductance of the leads and traces become significant, leading to transient or switching noise. These transients are related to the inductance of power/ground loop and hence this layout must be designed so as to reduce this inductance as much as possible. Hence, the layouts shown in Figure B4 give good and bad layouts for the power/ground interconnection.

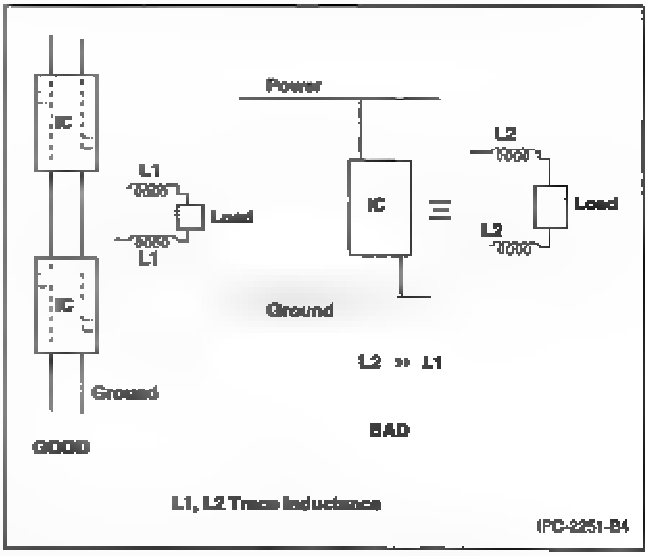


Figure B4 Power/Ground Interconnections

A common technique to reduce switching noise is the use of decoupling capacitors that serve to provide the current from a point closer to IC than the power supply. Even when this is done, the positioning of the capacitor is important, as shown in Figure B5. If the capacitor leads are too long, the self inductance becomes too high leading to the common switching noise.

The decoupling on DIP boards is normally achieved with discrete capacitors that can be closely positioned to the IC. For the higher I/O packages, a trend has started that is to

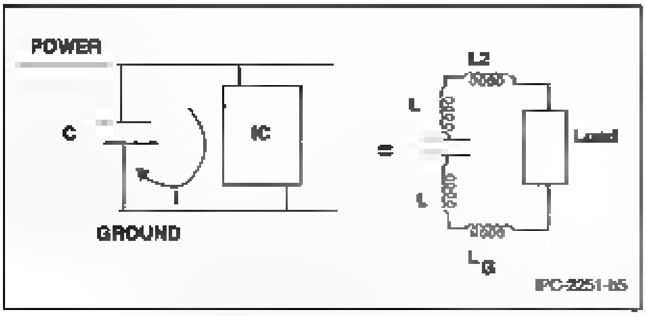


Figure B5 Decoupling Capacitor Placement

place the decoupling capacitor in the package as shown in Figure B6. This has the double advantage of not using real estate for the capacitor and reducing the size of the capacitor interconnections. Closely spaced adjacent power/ground planes are also being utilized to provide high frequency decoupling capacitance. This also decreases the real estate required for decoupling capacitors.

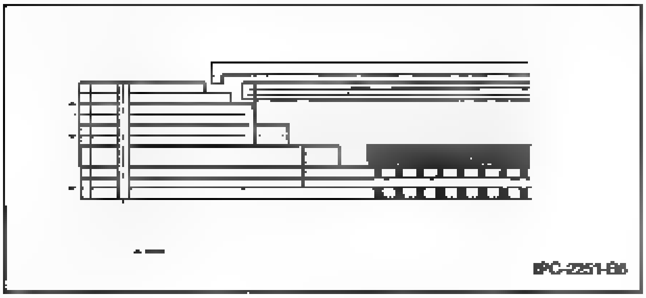


Figure B6 High I/O Component Decoupling Capacitor Design

B.3.4. Other Parasitics Noise Multilayer circuit boards have obvious advantages over double sided boards in the sense that the power/ground are continuous layers of metallization. Consequently, they offer a lower r.f. impedance to the spurious currents and the current distribution is such that the current in the return circuit follows the conductor wire path as shown in Figure B7.

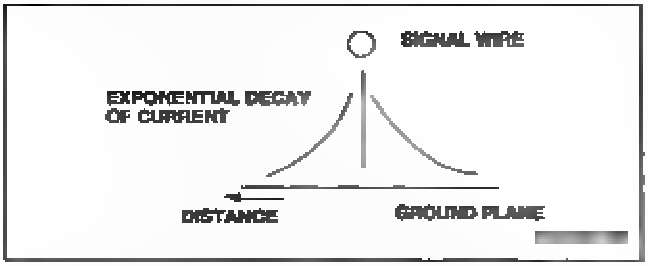


Figure B7 Current Distribution in Ground Plane

This means that the current loop is significantly reduced in area since the area is now bounded by the signal wire length and the separation between signal layer and the ground or decoupled power layers. To further enhance the multilayer improvement, adjacent layers (signal) can be run orthogonally thus reducing the crosstalk. The power and ground layers will also serve to shield emissions.

B.3.5 Noise Budget/Noise Margin In Section 5, we described the transmission line effects that interfere with the original electrical signal and modify it as it passes through the interconnection. This modification of the original signal may effect the performance of the system. But what are the limits in which the characteristics of the original signal can be modified and the system will continue to perform properly? This concept is called the "Noise Budget."

A noise budget is defined as the allocation of a voltage tolerance for the system DC and AC voltage drops for a device to operate within specific boundaries. There are two primary system noise budgets. The first is the DC power supply noise budget for each IC. The second is the device logic signal AC noise budget.

Each logic device connects to a positive voltage and a ground return. The system power distribution has finite AC and DC voltage drops between the power supply and component. Also, the power supply has a designated operating tolerance. The logic device must operate over an input voltage range of V_{CC} ± NM, where NM is the noise margin. The primary components that are allocated for the noise margin are:

a) Power supply tolerance

b) System DC drops

c) Bulk decoupling drops

d) IC decoupling drop

e) Component input voltage tolerance

f) Preset power supply voltage

These concepts are presented in detail in Chapter 5.

B.4 High Speed Electronics Packaging Design—Concept and Methodology We can conclude at this point with the fact that, if the requested digital signal speed is higher than the critical speed (as defined in Section 3.2), the transmission line effects interfere with the original signal creating delay and distortions. On the other hand, the capability of electronic devices to function properly when distorted signals and noises are propagated through the system is limited by their noise margin characteristics. A good packaging engineer must create a physical design in which the errors introduced by the transmission line effects are compatible with the noise budget of the system being created.

Although the concept sounds simple enough, one should not forget that a designer has to accommodate this requirement in a world in which another large number of restraints is already imposed from the type of system to design, from the technology to be implemented or simple limitations imposed by the material properties available in the market. These limitations leave to the packaging designer a narrow path in which he can find few options.

Appendix C

CIRCUIT BOARD LAYUPS

C.1 Common Printed Circuit Board Layups The following figures present typical multilayer printed circuit board layer constructions. These provide microstrip, stripline and dual stripline transmission line configurations. For optimum EMI performance, the highest frequency signals should be placed on internal layers below reference planes. Power distribution planes should be close to each other to provide maximum distributed capacitance for decoupling high speed signals.

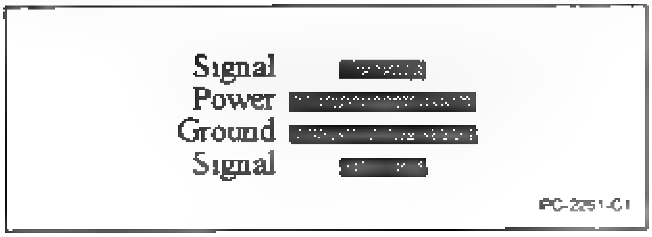

Signal
Power
Ground
Signal
IPC-2251-C1

Figure C1 4 Layer

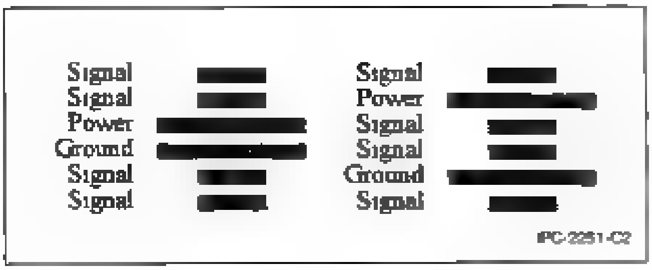

Signal
Signal
Power
Ground
Signal
Signal
Signal
Power
Signal
Signal
Ground
Signal
IPC-2251-C2

Figure C2 6 Layer

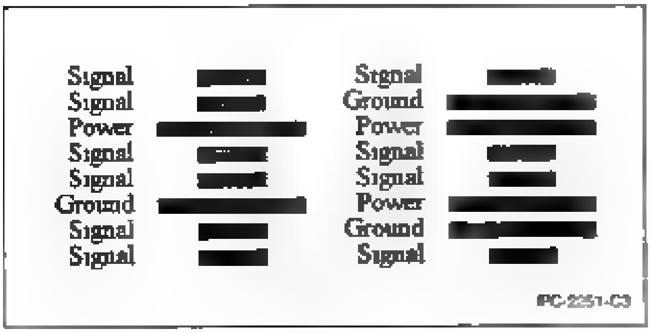

Signal
Signal
Power
Signal
Signal
Ground
Signal
Signal
Signal
Ground
Power
Signal
Signal
Power
Ground
Signal
IPC-2251-C3

Figure C3 8 Layer

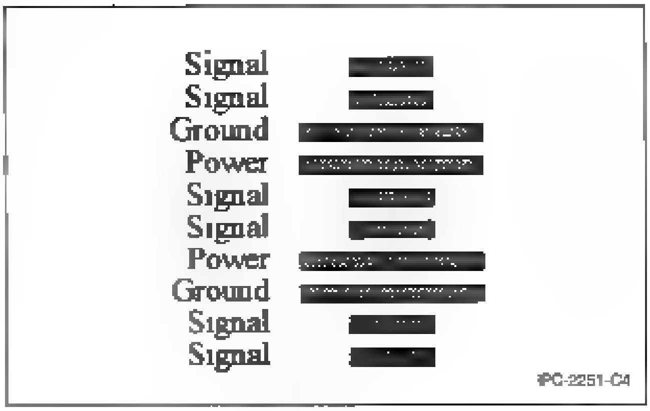

Signal
Signal
Ground
Power
Signal
Signal
Power
Ground
Signal
Signal
IPC-2251-C4

Figure C4 10 Layer

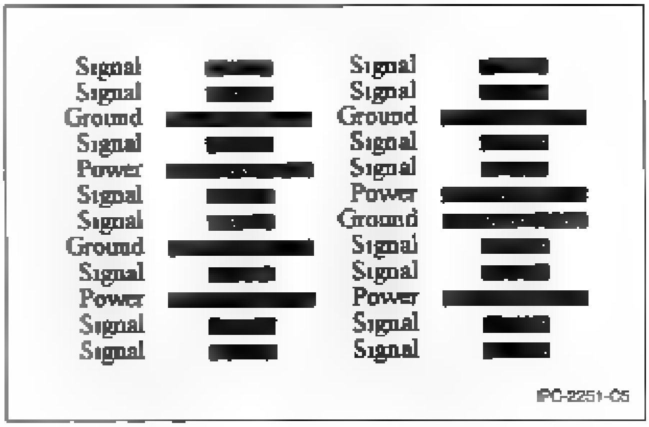

Signal
Signal
Ground
Signal
Power
Signal
Signal
Ground
Signal
Power
Signal
Signal
Signal
Signal
Ground
Signal
Signal
Power
Ground
Signal
Signal
Power
Signal
Signal
IPC-2251-C5

Figure C5 12 Layer

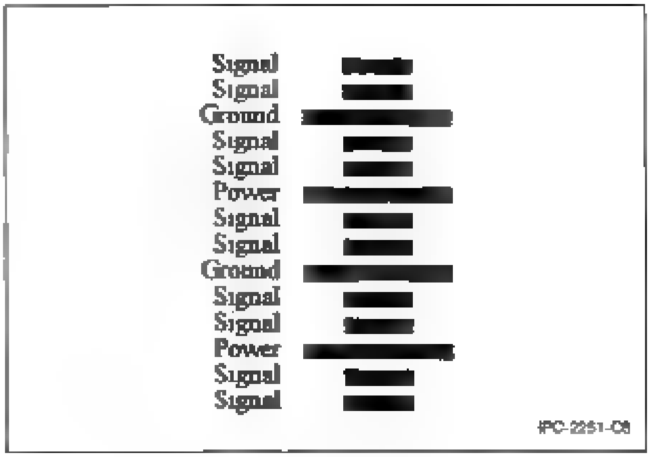

Signal
Signal
Ground
Signal
Signal
Power
Signal
Signal
Ground
Signal
Signal
Power
Signal
Signal
IPC-2251-C6

Figure C6 14 Layer

C.2 Common Discrete Circuit Board Layups The following figures present typical discrete wiring circuit board layer constructions. These provide microstrip, stripline and dual stripline transmission line configurations. For optimum EMI performance, the highest frequency signals should be placed on internal layers below reference planes.

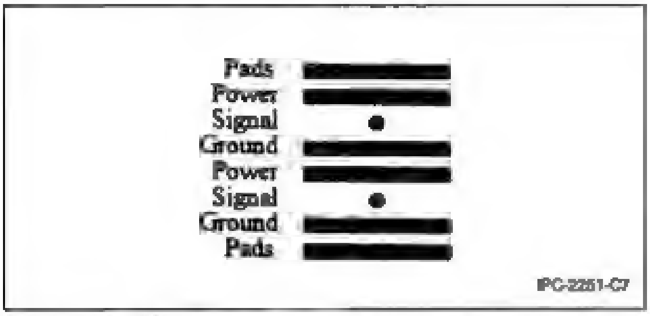

Pads
Power
Signal
Ground
Power
Signal
Ground
Pads
IPC-2251-C7

Figure C7 8 Layer

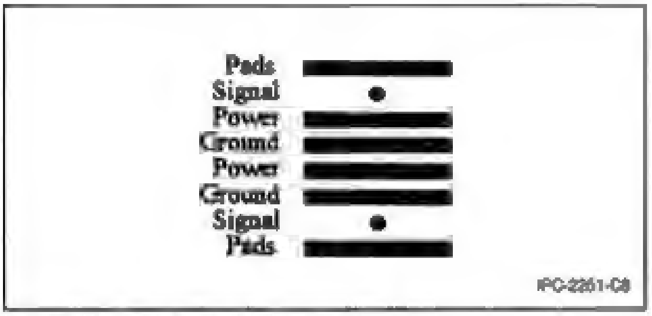

Pads
Signal
Power
Ground
Power
Ground
Signal
Pads
IPC-2251-C8

Figure C8 8 Layer; ML Core

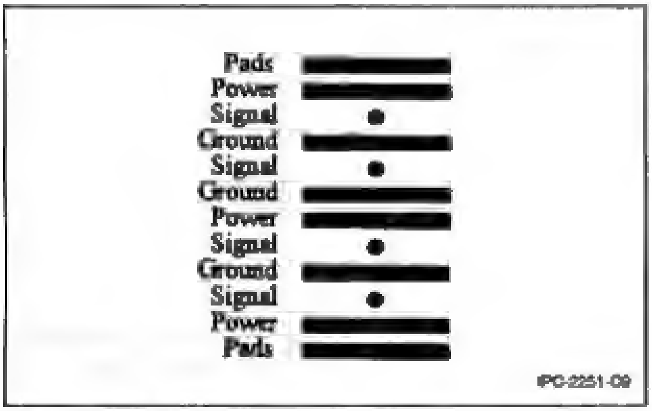

Pads
Power
Signal
Ground
Signal
Ground
Power
Signal
Ground
Signal
Power
Pads
IPC-2251-C9

Figure C9 12 Layer

Appendix D

BIBLIOGRAPHY

Impedance Calculation

G.L. Matthaei, et al., "Microwave Filters, Impedance-Matching Networks, and Coupling Structures," McGraw-Hill Book Co., New York, 1964, p. 168-196.

H. Howe, Jr., "Stripline Circuit Design," Artech House, Dedham, MA 1974.

J.P. Shelton, "Impedances of Offset Parallel Coupled Strip Transmission Lines," IEEE Trans., Vol. MTT-14, Jan. 1966, p. 7-15; Correction, MTT-14, May 1966, p. 249.

R.R. Gupta, "Fringing Capacitance Curves for Coplanar Rectangular Coupled Bars:, IEEE Trans., Vol. MTT-17, 1969, p. 637-638.

H.J. Riblet, "Two Limiting Values of the Capacitance of Symmetrical Rectangular Coaxial Strip Transmission Line," IEEE Trans., Vol. MTT-29, July 1981, p. 661-666.

S. Rimmon, "Master the Challenge of Offset Stripline Design," Microwaves, Vol. 15, May 1976, p. 40-44.

D.K. Larson, "Computer Plotter = Direct-to-Art Design," Microwave, Vol. 20, March 1981, p. 91-97.

H.E. Green and J.R. Pyle, Jr., "The Characteristic Impedance and Velocity Ratio of Dielectric Supported Strip Line," IEEE Trans., Vol. MTT-13, Jan. 1965, p. 135-136.

H. Howe, Jr., "Dielectrically Loaded Stripline at 18 GHz," Microwave Journal, Volume 9, Jan. 1966, p. 52-54.

J.K. Richardson, "An Approximate Formula for Calculating the Characteristic Impedance of a Symmetric Stripline," IEEE Trans., Vol. MTT-15, Feb. 1967, p. 130-131.

P. Schiffres, "How Much CW Power Can Striplines Handle?," Microwaves, June 1966, p. 25-34.

G.D. Vendelin, "Limitations on Stripline Q," Microwave Journal, Vol. 13, May 1970, p. 63-69.

Ashok K. Gorwara, "Transmission Media-What's Suitable at MM Wavelengths?" Microwaves, Vol. 15, March 1976, p. 36-42.

E. Yamashita and S. Yamayaki, "Parallel-Strip Line Embedded In or Printed On a Dielectric Sheet," IEEE Trans., Vol. MTT-16, Nov. 1968, p. 972-973.

E. Yamashita and K. Atsuki, "Stripline with Rectangular Outer Conductor and Three Dielectric Layers," IEEE Trans., Vol. MTT- 18, May 1970, p. 238-243.

J.M.C. Dukes, "An Investigation into Some Fundamental Properties of Strip Transmission Lines with the Aid of an Electrolytic Tank," Proc. IEE, Vol. 103, Part B, May 1956, p. 319-333.

J.M.C Dukes, "The Application of Printed Circuit Techniques to the Design of Microwave Components," Proc. IEE, Vol. 104, part B, 1957, p. 155-157.

A.F. Harvey, "Parallel-Plate Transmission Systems for Microwave Frequencies," Proc, IEEE, Vol. 106, part B, March 1959, p. 129-140.

H. Guckel, "Characteristic Impedance of Generalized-Rectangular Transmission Lines," IEEE Trans., Vol. MTT-13, May 1965, p. 270-274; Correction, MTT-16, Aug. 1968, p. 555.

E. Castamagna, "Fast Parameter Calculation of the Dielectric Supported Air-Strip Transmission Line," IEEE Trans., Vol. MTT- 21, March 1973, p. 155-156; Correction MTT-22, April 1974, p. 474.

C.M. Weil, "The Characteristic Impedance of Rectangular Transmission Lines with Thin Center Conductor and Air Dielectric," IEEE Trans., Vol. MTT-26, April 1978, p. 238-242.

H.R. Kaupp, "Characteristics of Microstrip Transmission Lines," IEEE Trans., Vol. EC-16, No. 2 April 1967.

Coupled Transmission Lines

H. Amemiya, "Time Domain Analysis of Multiple Parallel Transmission Lines," RCA Review, Vol. 28, No. 6, pp. 241-276, June 1967.

I. Catt, "Crosstalk (Noise) in Digital Systems," IEEE Transactions on Digital Computers, Vol. EC-16, No.6, pp. 743-763, December 1967.

S.B. Cohn, "Characteristic Impedances of Broadside Coupled Strip Transmission Line," IRE Trans., Vol. MTT-3, Oct. 1955, p. 29-38.

C.W. Davidson, "Transmission Lines for Communication," John Wiley and Sons, New York, NY, 1978.

J.A. DeFalco, "Reflections and Crosstalk in Logic Circuit Interconnections," IEEE Spectrum, Vol. 7, No. 7, pp. 44-50, July 1970.

R. Facia and A. Wexler, "Greenfield: General Purpose Transmission Line Simulator," Product Data Sheets, Quantec Laboratories, Inc., Suite 200, 281 McDermot Ave., Winnipeg Canada R3B OS9, 1988. (204) 943-2552.

B.L. Hart, "Digital Signal Transmission," Van Nostrand Reinhold (UK), Wokingham, Berkshire, England, 1988.

O.A. Horna, "Pulse Reflections in Transmission Lines," IEEE Transactions on Electronic Computers, Vol. EC-20, No. 12, pp. 1558-1563, December, 1971.

D.W. Kammler, "Calculation of Characteristic Admittances and Coupling Coefficients for Strip Transmission Lines," IEEE Trans., Vol. MTT-16, Nov. 1968, p. 925-937.

G. Metzger and J. Vabre, "Transmission Lines with Pulse Excitation," Academic Press, New York, NY, 1969

V.K. Tripathi, "Loss Calculations for Coupled Transmission Line Structures," IEEE Trans., Vol. MTT-20, Feb. 1972, p. 178-180.

R. Pregla, "Distributed Capacitances for Coupled Rectangular Bars of Finite Width," AEU, Vol. 25, Feb. 1971, p. 69-72.

S. Yamamoto, et al., "Coupled Strip Transmission Line with Three Center Conductors," IEEE Trans.. Vol. MTT-14, Oct. 1966, p. 446-461.

W.J. Getsinger, "Coupled Rectangular Bars Between Parallel Plates," IRE Trans. Vol. MTT_10, Jan. 1962. p. 65-72.

W.J. Getsinger, "A Coupled Strip-Line Configuration Using Printed Circuit Construction that Allows Very Close Coupling," IRE Trans., Vol. MTT-9, Nov. 1961, p. 535-544.

J.D. Horgan, "Coupled Strip Transmission Lines with Rectangular Inner Conductors," IRE Trans., Vol. MTT-5, April 1957, p. 92-99.

J.L. Allen and M.F. Estes, "Broadside Coupled Strips in a Layered Dielectric Medium," IEEE Trans., Vol. MTT-20, Oct. 1972, p. 662-668; Correction, MTT-23, Sept. 1975, p. 779.

I.J. Bahl and P. Bhartia, "The Design of Broadside-Coupled Stripline Circuits," IEEE Trans., Vol. MTT-29, Feb. 1981, p. 165-168.

A.G. D'Assuncao, et al, "Inhomogeneous Broadside-Coupled Striplines," 1981 MTT Symposium Digest, p. 218-220.

J. Singletary, Jr., "Fringing Capacitance in Stripline Coupler Design" IEEE Trans., Vol. MTT-14, Aug. 1966, p. 398: Correction, MTT-15, March 1967, p. 200.

V.K. Tripathi, "Asymmetric Coupled Transmission Lines in an Inhomogeneous Medium," IEEE Trans., Vol. MTT-23, Sept. 1975, p. 734-739.

I.J. Bahl and P. Bhattia, "Characteristics of Inhomogeneous Broadside-Coupled Striplines," IEEE Trans., Vol. MTT-28, June 1980, p. 529-535.

I.J. Bahl and P. Bhartia, "The Design of Broadside-Coupled Stripline Circuits," IEEE Trans., Vol. MTT-29, Feb. 1981, p. 165-168.

A. Feller, H.R. Kaupp, et al, "Crosstalk and Reflections in High-Speed Digital Systems," Proceedings—Fall Joint Computer Conference 1965, p. 511–525.

J. DeFalco, "Predicting Crosstalk in Digital Systems," Computer Design June 1977, p. 69–75.

IPC

ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

ISBN #1-580987-30-3

2215 Sanders Road, Northbrook, IL 60062-6135
Tel. 847.509.9700 Fax 847.509.9798
www.ipc.org